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VOICE OF THE ENGINEER

MARCH 1
Issue 5/2012
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ENGINEERING THE NEXT GENERATION OF STEM

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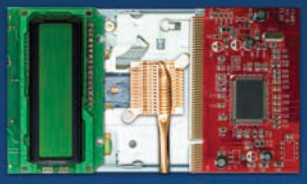
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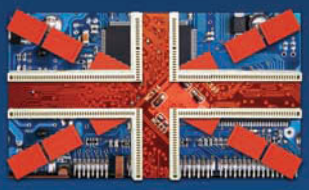
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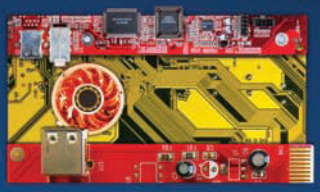
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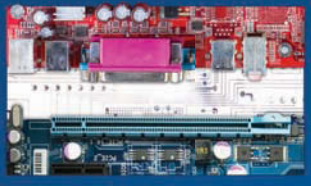
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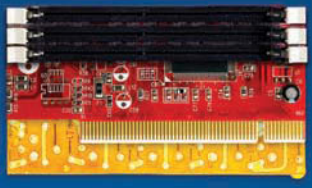
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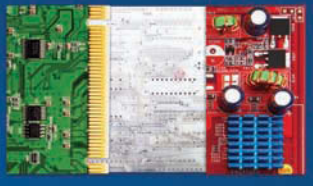
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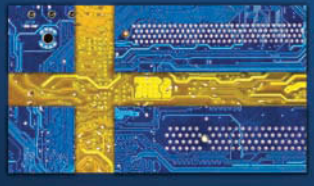
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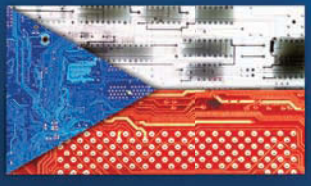
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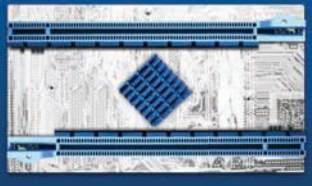
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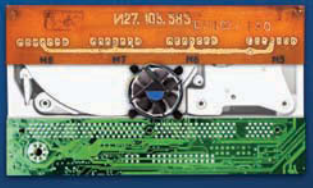
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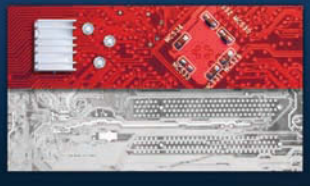
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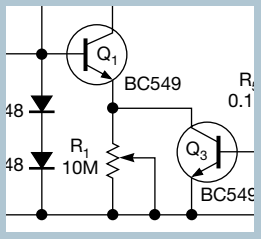

▶ Find out how to submit your own Design Idea: http://bit.ly/DesignIdeasGuide.

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DEPARTMENTS & COLUMNS

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Volume 57, Number 5 (Printed in USA).

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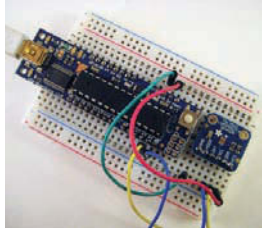
Comments, thoughts, and opinions shared by *EDN*'s community



In response to "Adafruit, Sparkfun point to the democratization of hardware," a blog post by *EDN*'s Margery Conner, http://bit.ly/xs0TeF, Chris G comments:

"The best thing about Sparkfun and Adafruit for a casual experimenter is that they offer components and subassemblies with most of the difficult work already done. Sure, the nitty-gritty details need to be understood before putting out a robust product, but, as my own efforts have shown, just trying to get a microprocessor to communicate to another device over I²C can be daunting enough while also working out the communication handshaking, even after reading the device maker's spec sheets. Having these things worked out in an experimenters' kit is the reason that these companies are the ones to watch."

In response to "Cow tipping," a Tales from the Cube column by Arnold N Simonsen, http://bit.ly/zaho6V, "bandit" comments:

"A moooving story, ranging by degrees from fence post to fence post. Our intrepid engineer bore-sighted right to the horns of the problem. The solution? Beefing up the trailer site, making hamburger of the problem, avoiding the cow patties in his path. Another government job properly steered away from danger."

DANIEL VASCONCELLOS

EDN *invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post. To review current comment threads on EDN.com, visit http://bit.ly/EDN_Talkback.*

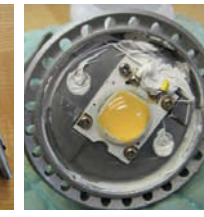
CONTENT

Can't-miss content on EDN.com

5 ENGINEERS: WHY DID YOU BECOME AN ENGINEER?

We asked, and you're answering. More than 185 comments have been posted so far, ranging from "I wanted to make the world a better place" to "The devil made me do it." Share what it was that inspired you to pursue engineering as a career path in this blog post's comment section.

http://bit.ly/yD1hsg



SAMSUNG LED-LIGHT-BULB TEARDOWN INCLUDES OBJECTIVE DIMMING NUMBERS

Samsung sent *EDN*'s Margery Conner an LED-replacement bulb to put through its paces and then tear down. How does the bulb do with the onerous TRIAC-dimming test? Pretty darned good, and Margery has posted a graph to prove it.

http://bit.ly/xEIkmE

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BY SUZANNE DEFFREE, MANAGING EDITOR, ONLINE

Do, make, design, build, and fix the future of STEM

By now, you've seen this issue's cover. You may have even flipped through to the cover story. And you may be wondering what such a story—sans schematics, technical jargon, and just plain design basics—is doing in *EDN*. We are about engineering, after all, so where's the engineering in the cover story? In this issue's cover story, instead of presenting a design topic for you to build from, we're presenting a challenge for all of us to overcome. That challenge is how to engineer a new generation of STEM (science/technology/engineering/math) talent.

We all know the problem. Too few new engineers, as well as other STEM professionals, are graduating from US colleges. The underlying issue is that kids these days aren't taking an interest in science and math, without which they can't develop critical-thinking skills and that sense of curiosity that contributes to entrepreneurial attitudes and life-long discovery.

Many people reading this editorial will say that we shouldn't be encouraging kids to study STEM because of a claimed lack of engineering jobs in the United States. This situation isn't just about jobs, though. It's about creating a climate of more creative and more intelligently thinking, and, ultimately, more proactive people. We can be sure of this: If engineers—who are creative, intelligent, productive people—ran things in this country, we'd all be in a better position when it came to the employment market, as well as many other hot-button concerns.

Engineering the next generation is about creating leaders who can help us build a better tomorrow. Although these leaders would preferably be new engineers, we also need more professionals in other fields, inside or outside STEM, who think like engineers to help brighten the picture.

It's easy to point fingers; politicians do it all the time. But, as engineers, you do, you make, you design, you build, and you fix. Those abilities—not the degree you received—make you an engineer. Those same principles make the topic of next-generation STEM talent an engineering issue. We know there is a problem. Let's do something to fix it; let's engineer it.

As issues about STEM evolve, you'll see more content like this cover story on how to engineer this crisis into a healthier state. This content will appear in print, on EDN.com, through our social-media efforts, in our webcasts, and through the events we attend. For example, *EDN* is presenting a Design West panel on this topic on March 28 at the San Jose McEnery Convention Center. Look for it in the show-floor theater at 1:30 pm. After the panel, we'll also host a networking session in which we'll invite experienced engineers and executives to connect with incoming and new STEM talent.

Further, the IEEE has asked me and my colleague at UBM Electronics, Naomi Price, online brand manager for Innovation Generation, to speak at its Integrated STEM Conference on March 9, at the College of New Jersey (Ewing, NJ). Naomi and I will also attend the USA Science and Engineering Festival in Washington, DC, during the last weekend in April to celebrate the brilliance this next generation brings to the game.

If engineers—who are creative, intelligent, productive people—were running things, we'd all be in a better position in the employment market.

We hope to see you at these events in March and April. You can find more information about them in the online version of this editorial. In the meantime, we invite you to share your own thoughts on what we can all be doing to help encourage the next generation of STEM at http://bit.ly/zC6wYA.

We'll bring back the design focus in *EDN*'s March 15 cover story. But don't walk away thinking that this need for more STEM talent isn't an engineering topic. It is vital to the future of engineering itself and something that we can together engineer—do, make, design, build, and fix—toward a better future. EDN

Contact me at suzanne.deffree@ubm.com.

IMAGE: THINKSTOCK

EDN

pulse

INNOVATIONS & INNOVATORS

Value-priced scopes extend bandwidth to 1 GHz

Agilent is adding four models to its InfiniiVision 3000 X series of value-priced digital oscilloscopes, doubling to 1 GHz the maximum bandwidth, increasing the maximum acquisition rate from 4G to 5G samples/sec/active channel, and adding such optional features as a ±3-digit digital voltmeter/five-digit frequency counter that uses the same signal leads as the scope. This option simplifies simultaneous numeric measurements and waveform display. The company has also expanded its Waveform Builder software line, which supports the built-in function/waveform-generator option. Memory depth is, optionally, 4M points/channel, and the maximum waveform-update rate remains 1 million waveforms/sec, a spec that only one competitor can equal without the use of special operating modes.

The wider bandwidth and increased acquisition rate position the new units, which include two- and four-channel analog scopes and mixed-signal oscilloscopes, to invade portions of the turf of higher-priced scopes. US list prices for 1-GHz-bandwidth units start at $9950 for a unit with two analog channels. According to Agilent, the 3000 X series' designed-in upgrade capabilities more effectively extend the instruments' lifetime and preserve users' investment than do competitive devices. Prices for upgrades from lower analog bandwidths to 1 GHz begin at $2340.

The company has also announced the $1000, 1-GHz N2795A active probe. The probe has one-quarter the input capacitance of passive probes that provide similar bandwidth. Although Agilent specs this device's bandwidth at 1 GHz, a company spokesman says that, when you use the 1-GHz probe with the 1-GHz scope, the combined –3-dB bandwidth remains higher than 1 GHz. The probe also sports a pair of LED "headlights" that make it easier to find probe points on dense PCBs. You can use one or two of these probes with a 1-GHz-bandwidth 3000 X scope. For applications that require both probing and 1-GHz bandwidth on more than two channels, the company recommends its 1157A probes, which draw less power from the scope's internal power supply.

—by Dan Strassberg

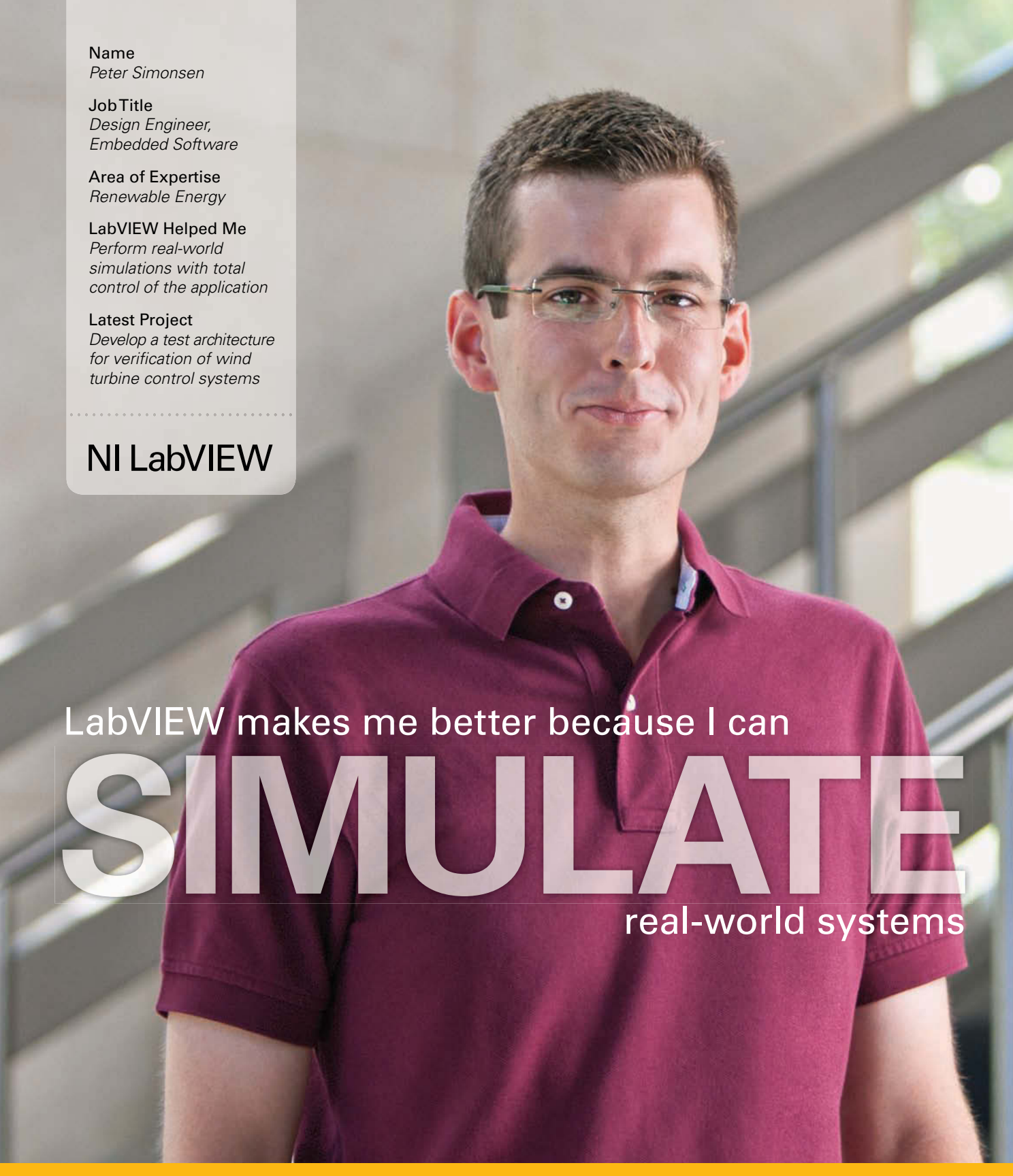
▷**Agilent Technologies**, www.agilent.com.

The four-channel MSO-X 3054A provides 1-GHz maximum bandwidth, 2M-sample/channel acquisition memory (4M samples optional), and 16 digital timing-analysis channels. A digital multimeter/frequency counter with on-screen readout, a built-in function/waveform generator, and a 1-GHz active probe are extra-cost options.

TALKBACK

"I became an engineer because I like clarity and specifics. I've learned from experience that, whenever a company avoids giving specifications, especially those involving price, be wary of fraud. Too many companies substitute [disreputable] marketing strategies for engineering transparency."

—*EDN* reader Neil Baker, in *EDN*'s Talkback section, at http://bit.ly/wLqanx. Add your comments.



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NATIONAL INSTRUMENTS™

Outdoor unit brings integration to the microwave backhaul

Broadcom's new BCM85810 microwave outdoor-unit IC combines the functions of as many as 10 off-the-shelf application-specific standard products, including IF and RF synthesizers, low-noise amplifiers, automatic-gain controllers, bandpass-filter banks, lowpass-filter banks, IR mixers, variable-gain and variable-voltage attenuators with automatic-gain control of more than 70 dB, and power-amplifier drivers and power detectors.

The BCM85810 fulfills the need for higher bandwidth in outdoor units.

The BCM85810 addresses the need for higher bandwidth and faster time to market in microwave split-mount and full- and all-outdoor units. With support for high modulation and with only two variants to cover all standard point-to-point microwave-frequency bands and channel bandwidths, the BCM85810 simplifies system manufacturing, deployment, and inventory management, according to the company.

The device offers an automatic-gain-control dynamic range of more than 70 dB, internal power controls, and on-chip-selectable baseband filters. It maintains receiver output power over the full input-power range and complies with European Telecommunications Standards Institute and Federal Communications Commission standards. **—by Fran Granville**

▷**Broadcom**, www.broadcom.com.

SOC enables measurement for high-power monitoring in industrial applications

Maxim's new Teridian-based, three-phase 78M6631 power-measurement system on chip embeds power monitoring into high-load applications. The self-contained and customizable system suits use in industrial panels and motors, solar-panel inverters, storage power supplies, and data centers. The device's embedded metrology engine includes a range of embedded energy diagnostics, including power factor, harmonic distortion, voltage sag, and voltage dip. The 78M6631 also provides better than 0.5% system accuracy across a 2000-to-1 dynamic range, enabling the use of the lowest-value shunt for the current sensor, thus reducing heat and parasitic-power loss.

Preloaded firmware supports both Delta and Wye three-phase applications, reducing both development costs and time to market. The 78M6631 SOC is available in a lead-free QFN package and sells for $5.78 (1000).

—by Fran Granville

▷**Maxim Integrated Products**, www.maxim-ic.com.

DILBERT By Scott Adams

03.01.12

HIGH-CURRENT STORAGE CHOKES COME IN ERU 20 CASE SIZE

TDK-EPC has extended the standard EUR 13 and ERU 25 series of Epcos power inductors with the new ERU 20 series. The devices have inductance values of 1 to 35 µH and a current rating of 93 to 50A. Their dc-resistance values range from 0.62 to 7 mΩ. The ERU case sizes suit use in high-current, low-voltage dc/dc converters, point-of-load converters, and multiphase modules. The design employs ferrite cores and flat-wire winding technology. Low core losses and efficient design with self-supporting winding permit ultra-compact dimensions and good storage density.

The inductors have a 21×21.5-mm² footprint and an insertion height of 9.8 to 14.2 mm, depending on type. The ROHS-compatible devices are also available in customer-specific versions. Applications include power supplies in telecommunications and IT systems and inverters for photovoltaic systems.

—by Fran Granville

▶**TDK-EPC**, www.epcos.com.


The ERU 20 series has inductance values of 1 to 35 µH and a current rating of 93 to 50A.

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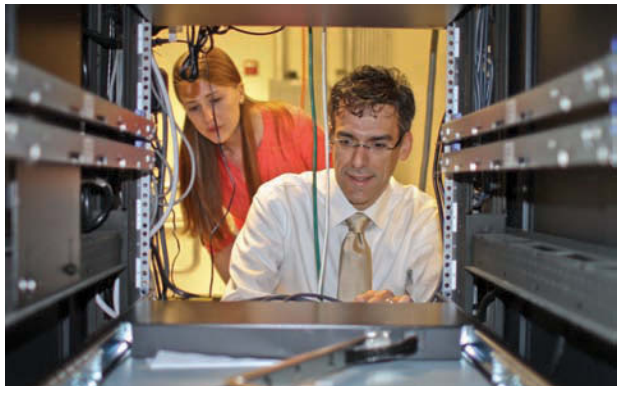
3-D computer simulations reveal diffusional behavior

A team of researchers at the Georgia Institute of Technology is exploring how nanoparticles move and diffuse on a surface or in a fluid under nonideal to extreme conditions. Rigoberto Hernandez, a professor at the university's school of chemistry and biochemistry, investigates these relationships by studying 3-D particle-dynamics simulations on high-performance computers. His findings focus on the movements of a spherical probe among static needles (**Reference 1**).

Hernandez and his former doctoral student, Ashley Tucker, assembled the rodlike scatterers in one of two states during his simulations: disordered, or isotropic, and ordered, or nematic. When disordered, the nanorods point in various directions and typically diffuse normally in all directions. When every rod points in the same direction, the particle, on average, diffuses more in the same direction as the rods than against the grain of the rods. In this nematic state, the probe's movement mimics the elongated shape of the scatterers.



Georgia Tech Professor Rigoberto Hernandez and his former doctoral student, Ashley Tucker, assembled the rodlike scatterers in one of two states during simulations: disordered, or isotropic, and ordered, or nematic.

Surprisingly, however, the particles sometimes diffuse faster in the nematic environment than in the disordered environment. That is, the channels left open between the ordered nanorods don't just steer nanoparticles along a direction; they also enable them to speed right through. As the density of the scatterers increases, the channels become more crowded. The particle diffusing through these assemblies slows dramatically in the simulation. Nevertheless, the nematic scatterers continue to accommodate faster diffusion than do disordered scatterers, according to the researchers.

"These simulations bring us a step closer to creating a nanorod device that allows scientists to control the flow of nanoparticles," says Hernandez. "Blue-sky applications of such devices include the creation of new light patterns, information flow, and other microscopic triggers." For example, if scientists need a probe to diffuse in a specific direction at a particular speed, they could trigger the nanorods to move into a specified direction. When they need to change the particle's direction, they could trigger scatterers to rearrange into a different direction. The trigger could even be the absence of sufficient nanoparticles in a given part of the device. The ensuing reordering of the nanorods would then drive a repopulation of nanoparticles that would then be available to perform a desired action, such as to stimulate light flow.

The National Science Foundation-funded work targets a better understanding of the motion of particles within complex arrays at the nanoscale. The work has significant long-term implications on device fabrication and performance at such scales.

—by Fran Granville

Georgia Institute of Technology, www.gatech.edu.

REFERENCE

1 Tucker, Ashley K, and Rigoberto Hernandez, "Diffusion of a Spherical Probe through Static Nematogens: Effect of Increasing Geometric Anisotropy and Long-Range Structure," *The Journal of Physical Chemistry B*, Dec 8, 2011, pg 1328, http://bit.ly/zFH6Yd.

Digital-audio processor integrates power management

Conexant's new dual-core, 32-bit CX20805 digital-audio processor integrates high-speed USB 2.0, an 800-MIPS DSP, and support for as many as eight endpoints. The chip comes with a C compiler, software tools, and a suite of DSP algorithms. It uses the vendor's CAPE (Conexant audio-processing-engine) architecture. Each dual-core DSP includes dual media-access controllers operating at 200 MHz. The CX20805 also includes 520 kbytes of embedded SRAM and 352 kbytes of embedded ROM; a full-duplex, I²S-multiplexed stereo with a four-channel PCM interface; an I²C master and slave; and an SPI master and slave.

Other features include support for a quad digital microphone with pulse-density modulation, SPDIF receiving and transmitting, tricolor PWM-LED drivers, and 24 programmable I/Os. A custom audio bus connects to multichannel audio devices, and the product has an AES 128 decryption engine, an on-chip logic analyzer and JTAG, a UART, and dedicated peripheral and memory-to-memory DMA channels. Integrated dc/dc conversion, power gating, power retention, dynamic voltage scaling, and frequency scaling reduce power consumption.

The CX20805 processor supports eight endpoints.

Housed in a 9×9-in., 116-pin, dual-row QFN package, the device sells for $5.50 (10,000). Evaluation kits are available to qualified customers and partners.

—by Fran Granville

Conexant Systems Inc, www.conexant.com.

Robust three-axis sensor targets automotives

STMicroelectronics' new A3G4250D angular-rate gyroscope aims to add position accuracy and stability to a range of automotive applications, including in-dash navigation, telematics, and vehicle-tolling systems. The AEC-Q1000-qualified gyroscopes provide accurate measurements of angular-motion detection, significantly enhancing dead-reckoning and map-matching capabilities in car-navigation and telematics applications.

By monitoring motion, distance traveled, and altitude, dead-reckoning systems compensate for the loss of satellite signals indoors and in urban canyons between tall buildings. Precise gyroscope readings also improve map-matching, the process of aligning a sequence of observed user positions with the road network on a digital map, such as those for traffic-flow analysis and driving directions.

The three-axis A3G4250D automotive gyroscope provides motion measurement along all three orthogonal axes.

The device employs one sensing structure for motion measurement along the orthogonal yaw, roll, and pitch axes, eliminating interference between the axes, increasing measurement precision, and providing output stability over time and temperature. The A3G4250D measures angular rates to ±250°/sec. An on-chip IC interface converts the angular motion into a 16-bit digital bit stream that transmits to a dedicated microcontroller chip through a standard SPI or I^2C protocol. The device provides interrupt and data-ready output lines and four user-selectable output-data rates.

The 3V-single-supply sensor integrates power-down and sleep modes and an embedded first-in/first-out memory block for power management. The A3G4250D embeds an 8-bit temperature sensor and operates at an extended temperature range of –40 to +85°C. The device is robust against EMI and withstands shocks as large as 10,000g. It sells for $6 (1000).

—by Fran Granville

▷**STMicroelectronics**, www.st.com.

03.01.12

Energy-measurement IC eases utility meters' transition to smart grid

Look out, you spinning-disk utility meters out there. Your days of ruling the power line are coming to a close—at least you'll get that impression as smart meters that employ electronic sensing to provide advanced connectivity continue to replace the venerable glass-encased meters that have served the utility industry for more than 100 years. The latest entry in the metering-IC arena is the CS548x/9x family from Cirrus Logic. The family supports single- and multiple-phase ac-line measurement of voltage and current through per-channel ADCs and then calculates the power usage using an internal digital core.

Other ICs for this application use SOC front ends and separate communications processors, but the topology of the Cirrus devices puts the converters and calculating core at the front end, lowering cost through the elimination of unneeded hardware blocks, according to the vendor, and using optocouplers, thus requiring fewer signal lines to isolate. Applications for these IC-based energy meters go beyond residential lines and their metering. Vendors are looking to incorporate them into appliances, smart power strips, power supplies, and power-hungry servers in enterprise applications.

The devices offer measurement accuracy for both active and reactive power (power factor) of 0.1% over a 4000-to-1 dynamic range, surpassing industry requirements, whereas current rms measurement accuracy is 0.1% over a 1000-to-1 range with readings using simultaneous-sampling converters and 24-bit, fourth-order delta-sigma modulators. On-chip measurements include active, reactive, and apparent power; rms voltage and current; power factor; and line frequency.

For transducer I/O—critical to this application—the ICs support shunt resistor, current transformer, and Rogowski-coil pickups, with configurable digital outputs for energy pulses, zero crossing, or energy direction. The chip's self-calibration time is less than 2 sec, which Cirrus claims is one-tenth the time of other available devices. Calibration time is important because these meters and their sensors require calibration at the factory's production line. At the other side of the I/O situation, the family offers SPI and UART interfaces, depending on IC model. The devices operate from a single 3.3V supply, and power consumption is less than 13 mW.

The CS548x/9x family includes two-, three-, and four-channel front ends, which are available in 16-lead SOIC, 24-lead QFN, and 28-lead QFN packages. Prices begin at 75 cents (100,000) for the smallest member of the family.

—by Bill Schweber

▶**Cirrus Logic**, www.cirrus.com.

BY HOWARD JOHNSON, PhD

Series resonance in power systems

Many digital systems suffer excessive power-supply noise at frequencies relating to the system clock. Could a series-resonant circuit, such as the one in **Figure 1**, connected between the power and the ground planes attenuate that noise? The answer can be yes, but only if your circuit satisfies the following improbable conditions.

First, the frequency of the system clock must remain fixed. In systems without a crystal-controlled clock, the clock frequency may wander ±30% or more. Low-power systems often slow the clock to conserve power when idle. High-performance systems sometimes come in speed variants, for which customers pay extra to gain performance. As a diagnostic test, a designer may slow the system clock to reveal certain timing-related failures. No power-supply-noise-mitigation strategy employing careful tuning of exact noise frequencies can possibly work under these conditions.

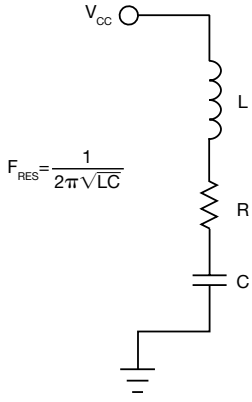


Figure 1 The impedance of this network attains its smallest value at the resonant frequency.

The allure of a series-resonant circuit is that it permits the use of a smaller value of capacitor than otherwise might be necessary *if* you match that capacitor with appropriate values of inductance and resistance, creating the series-resonant effect. Unfortunately, the smaller the capacitor, the more precise the circuit must become.

For example, a capacitor of one-fifth the ordinary value requires capacitor and inductor components with ±10% tolerance. A capacitor of one-tenth the normal value requires ±5% tolerance, and so on. It is difficult to implement high-frequency inductors with such tight tolerances. If you think of the layout inductance as fixed and plan a smaller value of capacitance to place the series-resonant point at a favorable location, you will face the same difficulty: You cannot easily control the exact values of capacitance and inductance.

The clock must play continuously, repeating forever without stops or gaps. If the clock stops, your resonant circuit will spin on, plunging out of control, creating disturbances just as bad as the problem you were trying to mitigate. When the clock restarts, the resonant circuit takes many cycles to catch up—providing zero benefit during that period. A resonant circuit is useful only with continuous stimulation. It is powerless to prevent noise from random data events.

You must place the series-resonant circuit within a small fraction of one wavelength of any device that it is protecting. Within that limited radius, the spreading inductance of the power and ground planes modifies the effective series inductance of the resonant circuit. Consequently, the exact positioning of a resonant circuit matters tremendously, so you cannot alter the layout without implementing a complete redesign. Even worse, a resonant element that provides substantial attenuation for clock noise emanating from one location may provide no benefit or may even exacerbate the noise from another source.

In a sinusoid-based system, such as an AM or an FM radio, resonating power-supply components can provide astonishing benefits.

Last, remember that a resonant circuit attenuates noise at only one frequency. It provides little or no benefit at other harmonics of the clock rate. In a sinusoid-based system, such as an FM or an AM radio, resonating power-supply components can provide truly astonishing benefits.

In a digital system that starts and stops at various clock speeds and in which the layout constantly changes from one version to the next, the use of resonating power-supply-filter elements does not pass the KISS (keep it simple, stupid) test. A digital-power system is better served by lots of large, simple, nonresonant bypass capacitors. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com, or e-mail him at howie03@sigcon.com.

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Look What's Happening at IMS2012!

Plenary Session Speaker: Steve Mollenkopf

President and Chief Operating Officer, *Qualcomm*

3G/4G Chipsets and the Mobile Data Explosion

Monday, 18 June 2012
1730-1900

The rapid growth of wireless data and complexity of 3G and 4G chipsets drives new design and deployment challenges for radio and device manufacturers along with carriers. This talk will provide a perspective on the problem from the point of view of a large, worldwide manufacturer of semiconductors and technology for cellular and connected consumer electronics devices. The increase in device and network complexity will result in significant business opportunities for the industry.

Closing Ceremony Speaker: Thomas H. Lee

Professor, *Stanford University*

The Fourth Age of Wireless and the Internet of Everything

Thursday, 21 June 2012
1700-1830

"Making predictions is hard, particularly about the future." The patterns of history are rarely discernible until they're obvious and perhaps irrelevant. Wireless may be an exception, at least in broad outline, for the evolution of wireless has been following a clear pattern that tempts us to extrapolate. Marconi's station-to-station spark telegraphy gave way to a second age dominated by station-to-people broadcasting, and then to today's ubiquitous people-to-people cellular communications. Each new age was marked by vast increases in value as it enlarged the circle of interlocutors. Now, these three ages have covered all combinations of "stations" and "people," so any Fourth Age will have to invite "things" into the mix to provide another stepwise jump in the number of interlocutors. This talk will describe how the inclusion of multiple billions of objects, coupled with a seemingly insatiable demand for ever-higher data rates, will stress an infrastructure built for the Third Age. Overcoming the challenges of the coming Fourth Age of Wireless to create the Internet of Everything represents a huge opportunity for RF engineers. History is not done.

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IEEE

BY PALLAB CHATTERJEE

Smart wireless for your world

Wireless for data transmission has been around for a long time and has slowly been creeping into computing devices in networks. Although RF interfaces were previously on IT and industrial-control systems, which had full-time management, the prevalence of high-performance embedded computing has created a need for distributed networks without full-time administration. This need exists independently of the platform you use—whether a microcontroller, a DSP, or a processor.

The digital-function and control side of the network has advanced to the point that it can address the self-handshaking and protocol negotiation necessary for these devices to both connect and identify themselves with minimal user intervention. A key portion of this task is the ability for the software and controller to manage the nonsequential turn-on and turn-off cycles of devices in the network as people move the devices to multiple locations and run multiple tasks without administration.

This control function is now influencing the RF side to move from individual power amplifiers, SAW (surface-acoustic-wave) filters, multiplexers, and low-noise amplifiers to full modules ranging from single-frequency transceivers to multiple-frequency cellular blocks. The resulting challenges in the RF area are spectrum crowding and the existence of multiple standards.

The RF spectra neatly divide into discrete data bands that all serve different system goals. These discrete functions, however, are all blending into the Internet of Things, which is growing daily (**Figure 1**). Most embedded computing devices are now transferring data to other applications and across spectra. This trend shifts the interoperability issue to the RF from the digital as reconstructed data becomes reconstructed data in the digital domain.

The common domains for the device networks are Z-Wave in the 900-MHz spectrum; Zigbee in the 2.4-GHz spectrum, which the IEEE 802.15.4 standard covers; Bluetooth, also in the 2.4-GHz band; WiMax, which the IEEE 802.16 standard covers and which supports PHY-layer devices from the 2- to 11-GHz and the 10- to 66-GHz spectra; and the mainstream wireless-data networks of Wi-Fi, under the IEEE 802.11 standards, which use multiple simultaneous data streams on the 2.4- and 5-GHz bands.

Manufacturers are integrating these device domains into peer-to-peer networks, mesh networks, LANs, and WANs. These networks supplement the multiple bands and protocols for cellular communication. Cell networks currently employ the 850-, 900-, 1800-, and 1900-MHz bands. All of these networks have made the digital shift to requiring little user intervention for communication, including automated handshaking, network connection, and device identification. The challenge for the end device is to determine which network to use. RF must appear in the end devices as a selection of one of multiple blocks.

A typical tablet PC with cellular connection may have more than seven RF-amplifier-transceiver blocks—four quad bands for the 3G cellular system, at least two blocks for 2.4 and 5G Wi-Fi bands, and one block for Zigbee or Z-Wave home- and industrial-automation network control and interface. The Wi-Fi blocks may support as many as four antennas, which the 801.11ac spec allows, and the RF must run in parallel.

The size, power, and module integration of the required bias, amps, filters, multiplexers, and multiple signal paths are driving the analog and RF community to move to its equivalent of an RF SOC. Manufacturers are releasing these devices with full signal conditioning, and they will soon include data-conversion and postsignal-recovery capabilities that are driving both the growth and the consolidation of the industry. EDN

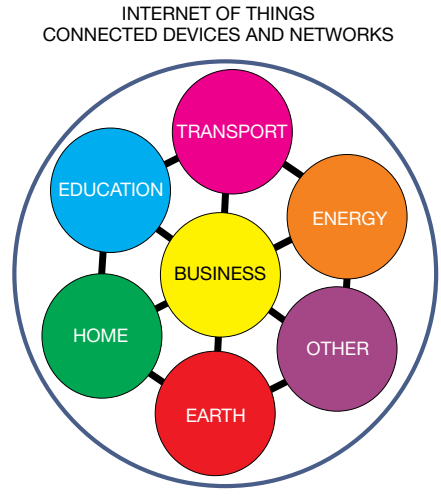

Figure 1 The RF spectra neatly divide into discrete data bands that all serve different system goals. These discrete functions, however, are all blending into the Internet of Things, which is growing daily.

Pallab Chatterjee has been an independent design consultant since 1985.

ADDRESSING CRITICAL-AREA ANALYSIS & MEMORY REDUNDANCY

HOW SUSCEPTIBLE IS YOUR DESIGN TO RANDOM DEFECTS, AND WHICH AREAS OF THE LAYOUT COULD BENEFIT FROM MODIFICATIONS THAT WOULD PROVIDE THE GREATEST POSITIVE EFFECT ON OVERALL YIELD?

BY SIMON FAVRE • MENTOR GRAPHICS

Design teams—whether using fabless, fablite, or IDM (integrated-device-manufacturer) processes—should handle the goal of reducing a design's sensitivity to manufacturing issues. The further downstream a design goes, the less likely it is that you can address a manufacturing problem without costly redesign. By promptly addressing DFM (design-for-manufacturing) problems when the design is still in progress, you can avoid manufacturing-ramp-up issues.

IMAGE: SHUTTERSTOCK

One aspect of DFM is determining how sensitive a physical design, or layout, is to random particle defects. The probability of a random particle defect is a function of the spacing of layout features, so tighter spacing increases random defects. Because memories are relatively dense structures, they are inherently more sensitive to random defects, so embedded memories in an SOC design can affect the overall yield of the device.

Understanding how to employ critical-area analysis becomes more important at each successive node. Memories keep getting bigger, and smaller dimensions introduce new defect types. The trade-offs that have worked well on previous nodes may give suboptimal results at the 28-nm node. For example, although manufacturers have avoided the use of row redundancy because they considered it too costly in access time, the technique becomes necessary at the 28-nm node so that vendors can achieve acceptable yields. All of these factors make careful analysis more valuable as a design tool.

AT A GLANCE

- The probability of a random particle defect is a function of the spacing of layout features. Because memories are relatively dense structures, they are inherently more sensitive to random defects, so they can affect the overall yield of the device.
- For a critical-area-analysis tool to accurately analyze memory redundancy, it must know the repair resources available in each memory block, a breakdown of the failure modes by layer and defect type, and which repair resource these modes are associated with.
- If you do not apply redundancy, then you may need to use alternative methods to improve die yield. These methods may include making the design smaller or reducing defect rates. If you apply redundancy in designs in which it has no benefit, then you waste die area and test time, increasing manufacturing cost.

CRITICAL-AREA ANALYSIS

Critical area is the area of a layout in which a particle of a given size will cause a functional failure. Critical area depends only on the layout and the range of particle sizes you are simulating. Critical-area analysis calculates values for the expected average number of faults and yield based on the dimensions and spacing of layout features and the particle size and density distribution that the fab measures. In addition to classic short- and open-circuit calculations, current practice in critical-area analysis includes via and contact failures. Analysis often shows that via and contact failures are the dominant failure mechanisms. You can incorporate other failure mechanisms into the analysis, depending on the defect data the fab provides.

Critical area increases with increasing defect, or particle, size. At the limit, the entire area of the chip is critical for a large-enough defect size. In practice, however, most fabs limit the range of defect sizes that they can simulate, based on the range of defect sizes that they can detect and measure with test chips or metrology equipment.

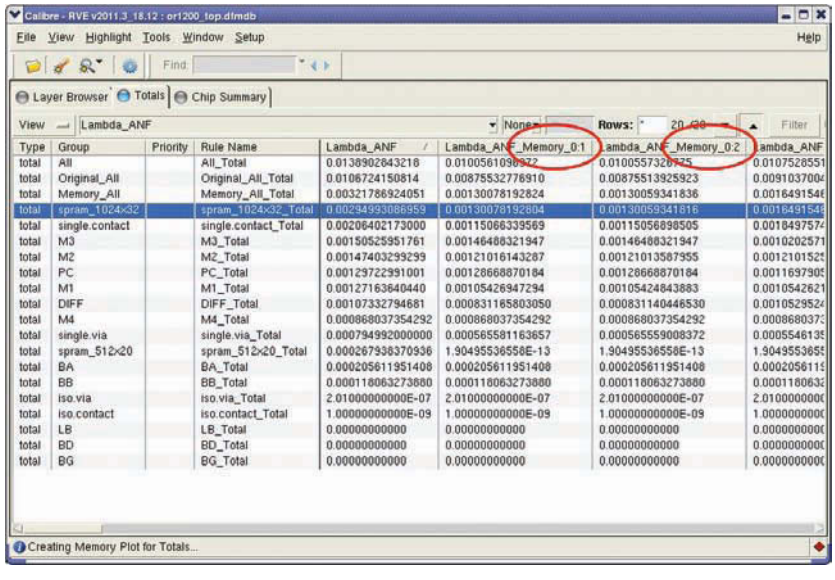

Figure 1 A critical-area analysis using Calibre shows the effects of memory redundancy on the average number of faults for different configurations.

DEFECT DENSITIES

Semiconductor fabs have various methods for collecting defect-density data. For use with critical-area analysis, the fab must convert the defect-density data into a form compatible with the analysis tool. The most common format is the following simple power **equation**: $D(X)=K/X^{Q}$, where K is a constant you derive from the density data, X is the defect size, and Q is the fall power. The fabs curve-fit the open and short circuits' defect data for each layer to an equation of this form to support critical-area analysis. In principle, a defect density must be available for every layer and defect type to which you will apply critical-area analysis. In practice, however, layers that have the same process steps, layer thickness, and design rules typically use the same defect-density values.

Manufacturers may also provide defect-density data in a table form that lists each defect's size and density value. A simplifying assumption is that, beyond the range of defect sizes for which the fab has data, the defect density is zero.

CALCULATING ANF, YIELD

To determine the average number of faults for a design, manufacturers use a tool that supports critical-area analysis, such as Mentor Graphics' Calibre, to extract the critical area for each layer over the range of defect sizes. To achieve this goal, manufacturers measure the layout and determine all of the areas in which a particle of a given size could result in a failure. The tool then uses numerical integration, along with the defect's size and density data, to calculate the

expected average number of faults, according to the following **equation**:

$$ANF=\int_{D_{MIN}}^{D_{MAX}} CA(X)\times D(X)DX,$$

where ANF is the average number of faults; D_{MIN} and D_{MAX} are the minimum and the maximum defect sizes, respectively, according to the defect data available for that layer; and CA(X) and D(X) are the critical area and the defect-density data, respectively.

Once the manufacturer has calculated the average number of faults, it is usually desirable to apply one or more yield models to make a prediction of the defect-limited yield of a design. The defect-limited yield cannot account for parametric-yield issues, so be careful when attempting to correlate this figure to actual die yields. One of the simplest and most common yield models is the Poisson model: $Y=E^{-ANF}$, where Y is the yield, E is a constant, and ANF is the average number of faults. It is generally simpler to calculate the average number of faults and the yield for cut layers, such as contacts and vias, than for other layers. Most foundries define a probabilistic failure rate for all single vias in the design and assume that via arrays do not fail. This simplifying assumption ignores the fact that a large enough particle can cause multiple failures, but it greatly simplifies the calculation of the average number of faults and reduces the amount of data the fab must provide. The designer needs only a sum of all the single cuts on a layer and can calculate the average number of faults as the product of the count and the failure rate.

MEMORY REDUNDANCY

Embedded memories can account for significantly large yield loss in SOCs due to random defects. Although SOCs can use other types of memories, assume that the design uses embedded SRAM. Typically, SRAM-IP (intellectual-property) providers make redundancy an option that designers can choose. The most common form of redundancy is the use of redundant rows and columns. Redundant columns are typically easier to apply because they address only the multiplexing of bit lines and I/O ports—not the address decoding.

To analyze failures with critical-area analysis, it is important to define which layers and defect types are associated with which memory-failure modes. By examining the layout of a typical six- or eight-transistor SRAM bit cell, you can make some simple associations. For example, by looking at the connections of the word lines and the bit lines to the bit cell, you can associate diffusion and contact to diffusion on column lines with column failures. Because contacts to diffusion and contacts to poly both connect to Metal 1, row and column layers must share the Metal 1 layer. Most of the layers in the memory design find use in multiple places, so not all defects on these layers will cause failures that are associated with repair resources. Irreparable, or fatal, defects, such as short circuits between power and ground, also occur.

REPAIR RESOURCES

Embedded-SRAM designs typically use either built-in self-repair or fuse

structures that allow multiplexing out the failed structures and replacing them with the redundant structures. Regardless of the method of applying the repair, the use of redundant structures in the design adds area, which directly increases the cost of manufacturing the design. Additional test time also increases cost, and designers may have a poor basis for calculating that cost. The goal of analyzing memory redundancy with critical-area analysis is to maximize defect-limited yield and minimize the effect on die area and test time.

A critical-area-analysis tool can accurately analyze memory redundancy only if it knows the repair resources available in each memory block, the breakdown of the failure modes by layer and defect type, and which repair resource these failure modes are associated with. Calibre can specify these variables as a series of critical-area-analysis rules. Each memory block also requires a count of total and redundant rows and columns. To identify the areas of the memory that can be repaired, you can either specify the bit-cell name that each memory block uses or use a marker layer in the layout database to allow the tool to identify the core areas of the memory.

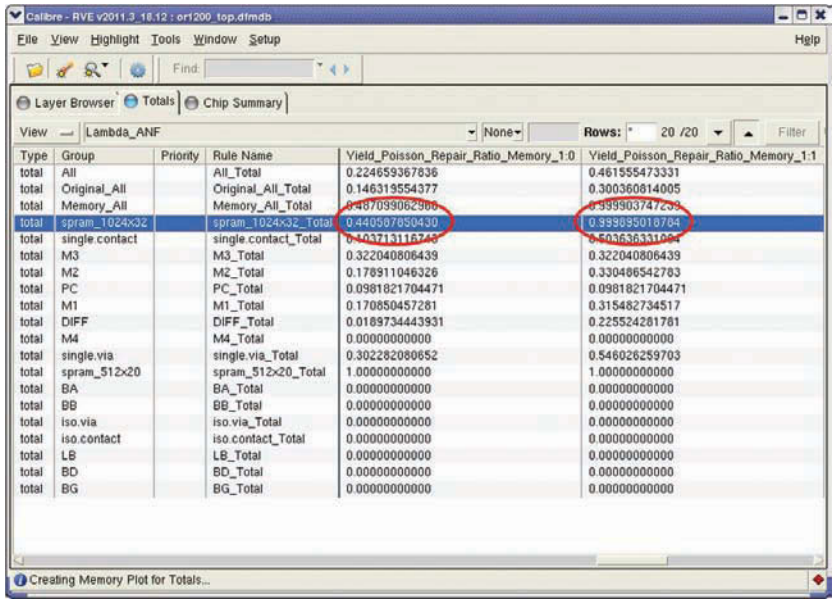

Figure 2 A critical-area analysis shows the memory-repair ratio for many parameters.

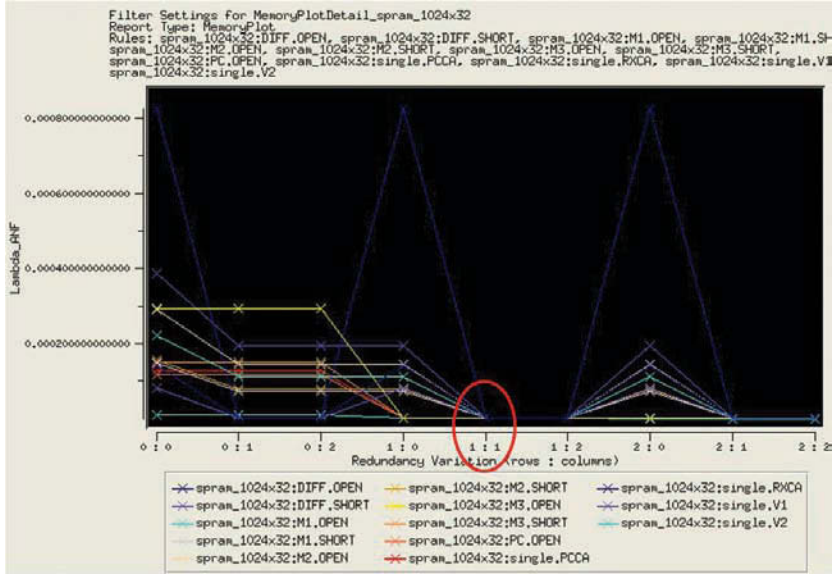

Figure 3 A memory plot shows the average number of faults for various memory-redundancy configurations. The combination of one redundant row and one redundant column causes a large decrease in the average number of faults.

Listing 1 provides the sramConfig memory-redundancy specification. The first two lines list the critical-area-analysis rules—that is, the type of defects that can occur—that have redundant resources for a family of memory blocks. The first two lines also contain the column rules and the row rules. These rules depend on the type and the structure of the memory block but are independent of the number of rows and columns and the redundancy resources. The last two lines describe an SRAM block design and specify, in order, the block name, the rule-configuration name, the total columns, the redundant columns, the total rows, the redundant rows, the dummy columns, the dummy rows, and the name of the bit cell. In this example, both block specifications refer to the same rule configuration, sramConfig. Given these parameters, Calibre calculates the unrepaired yield using the defect-density data that the fab provides.

YIELD WITH REDUNDANCY

Once the critical-area-analysis tool has performed the initial analysis, providing the average number of faults without redundancy, you can calculate the yield with redundancy. Calibre uses a calculation method employing the principle of the Bernoulli Trials, according to the following **equation**:

$$Y_R=\sum_{K=0}^{K=N_R} C(N_F,(N_F-K))\times P^{(N_F-K)}\times Q^K,$$

where N_F is the number of functional, nonredundant memory units; N_R is the number of redundant memory units; P is the probability of success, or yield, you derive from the average number of faults; Q is the probability of a failure (1–P); and $C(N_F, (N_F–K))$ is the binomial coefficient, which is a standard mathematical function. If the critical-

area-analysis tool can postprocess the calculations with different memory-redundancy specifications, it can present numeric and graphical output that makes it easy to visually determine the optimal amount of redundancy. The goal is to ensure the required number of good units out of a total number of units.

To see how effective memory redundancy can be, consider a hypothetical example. The memory of interest is a 4-Mbit, 32-kbit×128-bit SRAM. The goal is to realize at least 128 good units from a total of 130 units. In this case, there are two units needing repair and no defective units. Analysis determines that the unit yield considering one defect type is 0.999. The unrepaired yield of the entire core is then 0.999 raised to the 128th power, or 0.8798. If you perform the analysis for all defect types, the expected yield is approximately 0.35.

If you add redundancy to repair any unit defects, the repaired overall yield is 0.999. Memory designers use the repair-ratio metric to express the efficacy of memory redundancy. It stipulates that the repaired yield minus the unrepaired yield divided by one minus the unrepaired yield equals the repair ratio. A value in the high 90s is good. In this case, the repair ratio is (0.99–0.35)/(1–0.35), or 0.985.

Using Calibre to determine an optimum redundancy configuration, you must first set up a configuration file for the tool (**Listing 2**). The bit-cell name, ram6t, tells the tool the name of the hierarchical-layout element that describes a memory unit that can be repaired and that you should consider in this analysis. This name enables the tool to calculate the critical area of the entire memory core, including all instantiations of ram6t.

With this configuration information, Calibre calculates the average number of faults for memory with no redundancy, as well as for various redundancy configurations. **Figure 1** shows the results as a table with values of the average number of faults for different redundancy configurations. The table rows show the results for the entire design, for just the memory, and for specific types of defects. In the highlighted row, the average number of faults for the 1024×32-bit memory core improves substantially; the failure rate in Column 6 is half that in Column 5. To achieve this improvement, Column 6 includes one redundant row, but adding a second redundant row shows almost no further improvement (Column 7).

Figure 2 lists the effects of redundancy schemes in terms of repair ratio by design total, by total of all analysis layers, by memory, by block, and by layers or groups. **Figure 3** shows a tool-created plot depicting the average number of faults for each redundancy configuration and for each type of defect. The combination of one redundant row and one redundant column causes a large decrease in the average number of faults, and adding resources has little further effect. From these results, you can deduce that the expected average number of faults is based on the layout of the memory under consideration and the defect density of the fab and the process. The designer can now determine the effect of various redundancy configurations on the expected yield of an embedded memory.

Memory redundancy is intended to reduce manufacturing cost by improving die yield. If no redundancy is applied, alternative methods to improve die yield may include making the design smaller or reducing defect rates. If you apply redundancy to parts of the design in which it has no benefit, then you waste die area and test time, increasing manufacturing cost. Between these two extremes, you apply redundancy or not, depending on broad guidelines. Designs with high defect rates may require more redundancy; those with low defect rates may require no redundancy. The analysis of memory redundancy using critical-area analysis and accurate foundry-defect statistics is necessary for quantifying the yield improvement and determining the optimal configuration. EDN

LISTING 1 MEMORY-REDUNDANCY-SPECIFICATION EXAMPLE

```
sramConfig =
{ {DIFF.OPEN} {DIFF.SHORT} {single.ODCO} {M1 {0.4}}
  {single.VIA1} {M2} }
{ {PO.OPEN} {single.POCO} {M1 {0.4}}
  {single.VIA1} {M2} {single.VIA2} {M3} }

R128x32 sramConfig 34 2 128 0 0 0 ram6t
R2048x32 sramConfig 34 2 2048 0 0 0 ram6t
```

LISTING 2 CONFIGURATION ENTRIES FOR 4-MBIT SRAM

```
sramConfig =
{ {DIFF.OPEN} {DIFF.SHORT} {single.ODCO} {M1.SHORT}
  {M1.OPEN} {single.VIA1} {M2.SHORT 0.6}
  {M2.OPEN 0.6} }

{ {PO.SHORT} {PO.OPEN} {single.POCO} {M1.SHORT}
  {M1.OPEN} {single.VIA1} {M2.SHORT 0.4}
  {M2.OPEN 0.4} {single.VIA2} {M3.SHORT}
  {M3.OPEN} }

spram_2048x32_core sramConfig 34 2 2050 2 0 0 ram6t
spram_128x32_core sramConfig 34 2 130 2 0 0 ram6t
```


ACKNOWLEDGMENT

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AUTHOR'S BIOGRAPHY

Simon Favre is a technical-marketing engineer in the Mentor Graphics Calibre division, where he supports and directs improvements to the Calibre Yield Analyzer product. Before joining Mentor Graphics, Favre worked for Ponte Solutions, which Mentor acquired in 2008. He previously worked at other EDA companies, as well as at several semiconductor companies. Favre has bachelor's and master's degrees in electrical engineering and computer science from the University of California—Berkeley.

NI's Nicole Richard mentors in an elementary classroom.

ENGINEERING THE NEXT GENERATION OF STEM

INDUSTRY PARTICIPANTS, REACTING TO THE SO-CALLED ENGINEERING CRISIS, ARE DOING WHAT THEY CAN TO FOSTER SCIENCE, TECHNOLOGY, ENGINEERING, AND MATH TALENT AND ENCOURAGE MORE STUDENTS TO PURSUE ENGINEERING CAREERS.

BY SUZANNE DEFFREE • MANAGING EDITOR, ONLINE

The engineering industry is concerned about the lack of interest in STEM (science/technology/engineering/math) studies and careers from the youth of the United States. Some in the electronics industry refer to this concern as the "engineering crisis." The fear is that, as baby boomers exit the work force, there will be too few engineers to replace them. The problem has reached all levels of public acknowledgment—from President Obama's commenting on the need for STEM graduates in his January 24 State of the Union address to *Sesame Street*, which is incorporating more science and technology into its programming and which made "engineer" a word of the day in a September 2011 episode.

Despite these concerns, more undergraduate students graduated in 2011 than in 2010 with engineering degrees in all of the eight top engineering disciplines—aerospace, biomedical, chemical, civil, computer, electrical and electronic, mechanical, and nuclear (**Reference 1**). Yet, at a year-over-year increase of only 5071 new US bachelor's degrees in engineering for a total of 84,599 new degrees in 2011, the numbers are low, especially when you compare them with estimates from the President's Council of Advisors in Science and Technology describing a need for 1 million more STEM graduates over the next decade (**Reference 2**). Moreover, new degrees for electrical and electronic engineering declined from 2005's high of 14,742 through 2010's 11,968, only to inch up last year with an additional 37 degrees for 12,005 new degrees total in 2011.

Steve Lyle, director of education, work-force development, and diversity at Texas Instruments, admits that the number of engineering graduates is a concern. "The competition today for STEM talent is very, very tight in the United States," he says, noting that, although the unemployment rate remains generally high in the United States, the rate is below 4% for electrical engineers. "From an education standpoint, we [and our competitors] recognize that other countries—namely, India and China—are outpacing us in the number of engineers that are coming out of their universities."

TI, like many other electronics companies, isn't ignoring the problem. Instead, it's working toward a fix. The company has invested more than $150 million in STEM programs in the last five years and, like many others in the space, focuses its STEM efforts on student-achievement and teacher-effectiveness programs.

Like TI, Microchip Technology has engaged in STEM efforts through similar programs. "In the US political circuit, we often talk about the end product, which is jobs, but that [product] is the output of the rest of it," says Steve Sanghi, Microchip's president and chief executive officer. "We have to work on it well ahead of time and get kids excited about science, math, engineering, and technology. Corporations need to help nurture the resources and the community in which they operate. That [goal is] what we are trying to [achieve]: Prepare our future engineers; prepare our future employees; and educate the youth in math, science, engineering, and technologies."

Both Microchip and TI are proponents of FIRST (For Inspiration and Recognition of Science and Technology), an international program for children that combines hands-on, interactive robotics with a sportslike atmosphere and that provides more than $14 million in college scholarships. FIRST started in 1989 with approximately 20 teams. It has grown to more than 26,800 teams and currently reaches nearly 300,000 students. That growth is clear evidence that STEM can attract new young talent.

Microchip is the organizing sponsor of the FIRST Robotics Competition Arizona Regional, and Sanghi, who is also a member of the FIRST board of directors, notes that the competition had to turn away teams because of venue size. Next year, organizers may add a second competition or utilize a larger venue to accommodate more teams.

Carol Popovich, senior community relations representative for FIRST and Vex Robotics and a 16-year Microchip veteran whose full-time job is to work within the community on STEM, expects further expansion in the future. She notes a dramatic 30% growth in 9- to 14-year-old participants in the local FIRST Lego League in 2011 and anticipates that these young participants will continue to explore robotics as they enter high school. Popovich is one of approximately 40 Microchip employees involved in the competition. She describes the programs as having "a high fun quotient" that keeps not just the kids but also the sponsors and mentors returning each year.

AT A GLANCE

- Competition for STEM (science/technology/engineering/math) talent remains high.
- The industry is using several tactics, including robotics competitions, to spark students' interest in STEM.
- Mutual respect between mentors and mentees can lead to a rewarding experience for both parties.
- "Do engineering"—allowing next-generation talent the experiences of actual engineering, as opposed to theory-focused education—is a strong way to encourage interest in STEM.

MENTORING AND HIRING

Daniel Kinzer, a technical-support engineer who has worked at Raytheon for 28 years, started volunteering six years ago with his local high school's robotics club. The club's 40 students are spread over three FIRST Tech Challenge teams, which Raytheon sponsors. On a strictly volunteer basis, he spends four to five hours a week at Palm Harbor University High School (Palm Harbor, FL) during the building cycle and double that time, plus weekends, during competitions. "If I could retire, I'd do this full time," Kinzer says. "I'm not sure who's having more fun—me or the kids!"

Kinzer requires his teams to apply a full discipline to their projects. "The robotics portion isn't just robotics. It's mechanics, it's physics, it's programming, [and] it's engineering documentation," he says. "It's the difference between a bunch of kids molding things together until it works and [kids] really thinking out the process and identifying how things are going to work. Those are the types of abilities that [make you not only a] successful engineer but also successful in life." As a mentor, Kinzer recognizes that he is there to guide the students, not direct them. "I really don't like giving students ideas," he explains. "I only want [them] to expand on theirs. That [factor is] a key element of [being] a mentor."

Ed Smith, president of Avnet Electronics Marketing Americas, has previously mentored younger employees and interns at the company and has also tried to develop next-generation talent as a former president of the National Electronics Distributors Association Education Foundation. Smith advises mentors to listen more than they talk when working with their students. He also reminds mentors to be cautious of time commitments when entering a mentoring relationship. Recognition that the student's time is as valuable as the mentor's time is significant. "Don't do it unless you have the right amount of time," says Smith. "If you don't have the right amount of time, it really frustrates [the mentees]. They don't feel important."

Respecting the importance of the mentees, not only about their available time but also about the value of their ideas, goes a long way and is key to a rewarding experience for both parties. "A lot of these students tend to take us under their wing, as well," says Stewart Christie, product-marketing engineer in the intelligent-systems group at Intel. Christie works with interns at Intel; is engaged in student robotics and STEM activities at local schools; and often acts as a judge and a mentor in student competitions, including this spring's Cornell Cup, a college-level embedded-design competition. Intel and Tektronix sponsor this competition, which gives teams the opportunity to win as much as $10,000 (**references 3** and **4**). "It's great to have the fresh perspective and a much younger outlook than some of

us here have [at the office]. It's a mutual respect," Christie says.

"We who have been in the work force for a long [time] don't appreciate that what took us awhile to learn these young kids seem to have in their genes," says Pranav Mehta, senior principal engineer and chief technology officer for the intelligent-systems group at Intel. "It is amazing how advanced they are. If you just point them in the right direction, the kind of results that they can produce is mind-boggling. Many of my years-old assumptions shatter in seconds. Knowledge of society and the collective conscience has advanced to a point where these kids just see things that some of us cannot."

That excellence has encouraged Intel, as well as Avnet and TI, to hire many of its mentored interns. The companies often bring in young talent through internships or cooperative arrangements and then place them into rotational programs, allowing them to test-drive several design and business units. "As you increase the number of students coming in from college campuses, it's more important to have very robust development programs," says TI's Lyle, who notes that even TI's current chief executive officer, Rich Templeton, started at TI on a rotational basis. "We want to expose them to as many aspects of TI as possible so that they feel like they are getting a good start at the company."

The companies rarely work a continued mentoring responsibility into job descriptions, but, as Lyle says, "Part of being a leader is leading people. Part of leading a group is either directly providing that mentorship or ensuring that individuals in the organization, especially your high-potential talent, have the proper mentorship. It's not necessarily written down in everyone's job description, but it is understood that [mentoring] is an important part of leadership."

GETTING ON THE STEM PATH

Chris Gammell, a 28-year-old analog engineer, didn't wander into STEM until a high-school physics class sparked an interest. "My high-school physics teacher was really engaging," he says. "That set it off. I was always a science geek, but I had never done electronics before that. That's a big problem.

"My first digging into circuits was a co-op, and I just kind of hacked along," Gammell explains. "I'm a big proponent of co-ops. That's where I really learned how to solder. Someone finally sat me down and said, 'You're doing this wrong; let's show you how to do this.' There are a lot of engineers like that. As long as you actually want to listen and learn and you aren't egotistical about it, mentors are around and are gold."

Mentoring college students, interns, and entry-level employees helps cement STEM interest and give rise to young careers—a necessary effort because 45% of students who receive engineering degrees are not practicing engineers 10 years later, according to the ASEE (American Society of Engineering Education). But tapping interest at a younger age is important, as well. "[Kindergarten to Grade 12] is where it all starts," says Susan Donohue, general co-chairwoman of the IEEE Integrated STEM Education Conference, program chairwoman elect of the ASEE K-12 program, and lecturer at the University of Virginia School of Engineering and Applied Science. "If you [shortchange] them at the K-12 level, it's going to be so hard for them to catch up, and we can't afford to lose anybody."

Donohue has for several years been presenting engineering-teaching-kit workshops through the ASEE and Frontiers in Education. These kits include such tools as lesson plans, objectives, worksheets, bills of materials, and project materials, when possible. The self-contained kits enable teachers to open them and immediately bring more STEM into the classroom.

National Instruments has also taken steps to bring more STEM directly into the K-12 classroom. "We've had data come in that suggests that, if we don't have [children] interested before seventh and eighth grade, the likelihood

JOIN THE CONVERSATION

EDN recently asked its online readers what they could do each day to help inspire more interest in STEM. Share your answer and review other responses from your peers at **http://bit.ly/zC6wYA**.

The "Spectacular Seven" team from Oak Canyon Junior High in Lindon, UT, was the winner of the iGen fall 2011 LED Challenge.

[that they will go] into an engineering career is less," says Amanda Webster, community-relations manager at NI. For that reason, NI partners with Lego Group for educational robots and includes work with the FLL (FIRST Lego League) among its STEM and mentoring activities. FLL is an alliance between FIRST and the Lego Group that uses robotics to ramp up excitement about STEM at an earlier age than the FIRST Robotics Competition or FIRST Tech Challenge.

"I don't think that Dr T, our founder, thought that, years down the road, this high-tech company would be partnering with this toy company. But, with Lego being a top brand … , it has been a huge opportunity for us to get into the K-12 space," says Webster. "[Lego] lends credibility when you are standing in front of a 7-year-old trying to get him or her interested in math and science concepts that, unfortunately, even young children are showing a disinterest in."

When looking at root causes of the lack of interest, NI finds that a lot of teachers are either not interested in this area or feel that this area is not their strong suit. "We don't have a lot of EEs graduating and then going back to teach elementary school," Webster explains. "Our society has built up this dynamic [of not encouraging STEM to younger children. So] more than 150 [NI] employees go in, week after week, to the same classroom with the same teacher and students. As they go in every week, [they become] role models."

In the past, NI teamed with local universities to train its employees before they entered classrooms and began mentoring. Currently, the company hosts its own technical training for mentors and relies on teachers to help set expectations for the mentor's role in the classroom. "The training helps, but there is certainly a little trial by fire," Webster says. "By session two or three, the kids know them, and they become superheroes in the classroom. So it's just getting past that barrier and fear of going in."

That fear can be a major barrier when a STEM professional considers entering a classroom or working one on one with next-generation talent as a mentor. "After all, we are talking about science and engineering, and these systems can be very complex," says Dave Wilson, academic-relations director at NI. "But we have to take small steps and be willing to have something not work. While these things can be daunting, the technology is really reaching a point where it helps out a lot. Just try it."

"DO ENGINEERING"

One of the best ways to encourage interest in STEM is to let children actually engineer or, as Naomi Price, online brand manager for Innovation Generation, says, "let them get their hands dirty." Innovation Generation, or iGen, is a Web site that aims to develop excitement about STEM for the K-12 segment. UBM Electronics, the parent company of *EDN*, owns iGen, which hosts LED challenges that see student teams design and build based on a provided kit. For the fall 2011 iGen LED Challenge, the sponsored kit had a value of approximately $150 and included LEDs and a microcontroller. Students blog about their progress as their projects move along. In January, iGen named the "Spectacular Seven" team from Oak Canyon Junior High (Lindon, UT) as the winner of the fall challenge. The seven girls on the team, along with their teacher and their mentor, built a small Christmas tree made from PVC (polyvinyl-chloride) piping and loaded with flashing LEDs on the branches and a star on the top that flashes a countdown sign. "We're seeing a lot of energy from these kids," Price says, commenting on all of the teams who entered the challenge. "They are actually building something, and that [step] is important."

As part of its STEM efforts, MathWorks emphasizes hands-on, project-based learning. "I see more and more professors looking to integrate projects into their classrooms to get students excited and get a better understanding of what they are actually going to be doing when they graduate," says Tom Gaudette, principal education evangelist at the company. MathWorks has had close links to academia since its inception; its first customer was the Massachusetts Institute of Technology. Part of the company's support for project-based learning comes from its work on an integrated curriculum that includes its tools, as well as its work to provide support materials for those tools, such as free video tutorials.

The company works with universities to incorporate these tools, starting in basic classes and throughout the education process, so that students spend less class time on tool review and more on theory and lab work. "Having those base learning classes where students come in and are able to touch and feel and try to program a robot or try to control something gives the student a better idea of what it is to be an engineer versus freshman classes [such as] calculus, where they may not get the insight into what it is to be an engineer," Gaudette says.

MathWorks also supports hands-on engineering through EcoCar 2, a three-year competition during which engineering students design and build environmentally friendly vehicles. MathWorks equips all 16 participating university teams with its tools for model-based design, including Matlab

and Simulink. "EcoCar is teaching that process where you … do the design work and go through all the way to the last year of the competition, where you actually have a car driving around with the algorithms that the students created running on systems," Gaudette says. "That [achievement is] pretty impressive for undergraduate students. [When they graduate], they can say, 'I built a car, and I was part of a team that worked and did it all.'"

NI's Wilson reiterates this need for actually engineering to attract new engineers: "Theory is important. Simulation has its place, but, at some point, we honestly believe that a big answer to the question of how to attract, inspire, and ultimately mint new scientists and engineers is to give them the experiences and do engineering—not only theorize about it, not only conceptualize it, and not only simulate it. Those are parts of a process that have to culminate in the 'do-engineering' experience. If we can give relevant, exciting, real, experiential elements to students, the response can be very good."

Supporting that view, NI offers reasonably priced versions of its university- and student-targeted tools—ELVIS (Educational Laboratory Virtual Instrumentation Suite) and myDAQ (data-acquisition). ELVIS, a LabView-based design and prototype platform for universities, has midpoint prices of approximately $2000; myDAQ, a student-owned measurement-and-control tool that is slightly bigger than an iPhone, has student pricing as low as $175. "[The myDAQ tool] gives extensibility of the lab time to the students so they can experience the instrumentation as well as create their own instrumentation anyplace in or outside the lab," Wilson says. "We're seeing little back rooms and small areas with a table suddenly becoming labs because students can walk in with their laptop, myDAQ, and a little accessory board; plug in; and do their labs right there."

With lab time often scarce, such nooks of engineering practice are becoming more commonplace on college campuses, as well as elsewhere. As the "maker movement" continues rising with, as Gammell describes, "a resurgence of electronics and kits," so do hacker spaces. "I never realized that the students who come to these [hackerspace] meetings aren't allowed to solder in the dorms," says Intel's Christie. "They have to have a place to go where it is safe for them to use power tools and those sorts of equipment. Often, those tools are not available at the university."

SIGNAL RECEIVED

The need for more next-generation skilled STEM professionals is on the radar of companies and individuals, and, as such, they just may beat the engineering crisis. Still, much more effort is necessary. "We all need to participate in this [effort]," says NI's Wilson. "We need not to be so focused on the fact that there is a problem. We've figured that out. Now, let's challenge ourselves to bring our best ideas to the table. And let's set the bar—for pricing, accessibility, functionality, and ease of use for educators. If we do that, everyone will respond. But a fully defined problem is a half-solved problem. We need to start with the challenges. Once the constraints are clear, people will be really creative on how to solve them."EDN

Members of The Ohio State University team pose with their EcoCar vehicle.

MARK YOUR CALENDAR

for these upcoming STEM events:

- IEEE Integrated STEM Education Conference, March 9, 2012, at The College of New Jersey in Ewing, NJ
  http://bit.ly/wZH08o
- "Engineering the next generation of STEM" panel session and networking event at Design West, San Jose, March 28, 2012
  www.ubmdesign.com
- Second USA Science and Engineering Festival, April 28 to 29, 2012, Washington, DC
  http://bit.ly/xZtX1N

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BY IAN DENNIS • PRISM SOUND GROUP

Audio-converter-subsystem design challenges in the 21st century

SOME KEY STRATEGIES ENABLE YOU TO ACHIEVE OPTIMUM AUDIO-CONVERTER PERFORMANCE.

The habitat of audio converters is ever-changing. Designers built early converters into stand-alone digital-audio equipment. Later, they built them as stand-alone conversion devices with dedicated digital-audio connectivity. Nowadays, converters are increasingly available as peripherals for PCs or computer networks. Meanwhile, performance targets have been rising. In some ways, these changes have affected audio-converter design; in other ways, it's business as usual.

It seems that the plan of campaign for most engineers setting out to design an audio-converter subsystem—that is, a stand-alone converter or that part of the equipment that deals with audio conversion—is as follows: First, choose a data-converter device—an ADC, a DAC, or a codec chip—which will meet the project's requirements for performance, channel count, cost, and features. Then, implement a design around the device using the manufacturer's application note plus whatever additional features and interfaces the design requires. Most converter subsystems, however, either always or sometimes perform somewhat below the potential of their chosen data converter—usually because of several issues: clocking, unruly switch-mode power supplies, low-quality analog-signal paths, lack of attention to the voltage reference, and digital parts that go awry.

When digital audio was new, the data converter itself was almost the only consideration because it was impossible to build one with as much dynamic range and linearity as the professional or high-end consumer user required in analog equipment. Designers asked only, "What chip is in it?" Nowadays, workmanlike data converters can exceed a dynamic range of 130 dB and total harmonic distortion plus noise of 110 dB rms, unweighted, in the audio band. The weak link in a conversion system is most often elsewhere. No case exists for applying design effort or budget to the data converter itself, except in the most exacting of applications, and where it has already been applied in great measure to the rest of the converter subsystem. To get the best from your chosen data converter, you must apply painstaking design and relentless assessment.

TYPICAL ADC AND DAC SUBSYSTEMS

Figures 1 and **2** show typical ADC and DAC subsystems. You must take special care of the analog bits; several parts of the subsystem will try to make that task difficult. A dashed line indicates where you might consider isolating the analog and

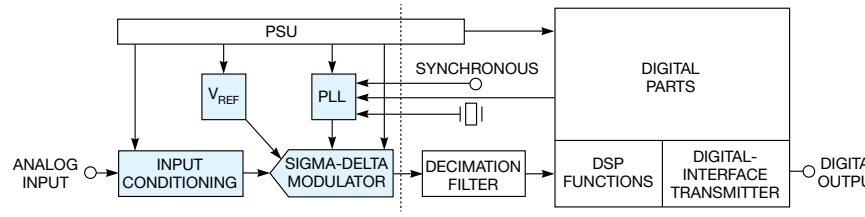

Figure 1 In a typical ADC, you must take special care of the analog bits (blue shading); several parts of the subsystem will try to make that task difficult.

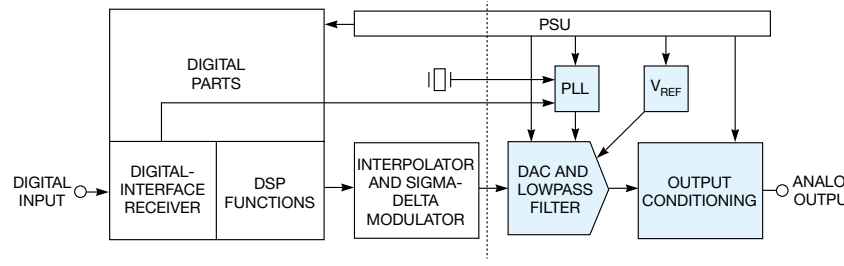

Figure 2 In a typical DAC system, the dashed line indicates where you might consider isolating the analog parts (blue shading) and the digital parts, but many ways are available for doing so, or you can opt not to isolate the parts.

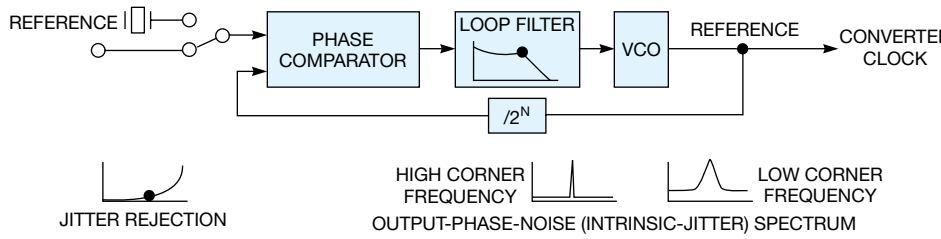

Figure 3 You might use a conventional analog PLL to lock a converter to a reference clock.

the digital parts, but many ways are available for doing so, or you can opt not to isolate the parts.

CLOCK RECOVERY

The conversion clock of a data converter is critical to its linearity because any variation in the regularity of the clock results in sampling jitter, which causes phase modulation of the converted signal (**Reference 1**). You can most easily assess this parameter by passing a high-amplitude, high-frequency signal through the converter and looking for phase-modulation sidebands or skirts in the spectrum of the output.

Converter clocks are usually derived from phase-locked loops rather than local oscillators; it is unusual for a device to be able to always be the system-clock master. It must be able to lock to an external reference or to its digital-audio or computer interface. To lock to all references, the lock range may need to be as wide as ±1000 ppm and must usually accommodate different sample rates (**Reference 2**).

The need to lock converter clocks to various wide-ranging references and to maintain low jitter tends to be among the most difficult challenges in converter design because it embodies some tough trade-offs. Although other applications, such as telecommunications, had somewhat solved this problem before digital audio emerged, audio engineers had to start from scratch, and it's taken a couple of decades to reinvent a good approach. The situation has become more challenging now that you must lock to software-generated syncs and time stamps arriving over computer interfaces because they can embody large amounts of jitter with uncontrolled spectrum and may not come around as often as you'd like (**Reference 3**).

Figure 3 shows a conventional analog PLL that you might use to lock a converter to a reference clock. A phase comparator continually compares the external reference with the regenerated version, and decides whether you should speed up or slow down the voltage-controlled oscillator to make them match in frequency and phase. You need to respond in a leisurely fashion; otherwise, you'll track any incoming jitter. Smooth out the up/down requests with a lowpass loop filter before passing them to the control input of the VCO.

The tough trade-offs, however, are mostly about choosing the right loop-filter characteristics and the right VCO. The design must reject incoming jitter down to low frequencies so that it does not become prey to audible sampling jitter. That requirement also potentially allows you to accommodate a low comparison frequency, such as a reference comprising infrequent software time stamps or a video sync that lines up with an audio sample only every few seconds.

Unfortunately, a low loop-filter corner frequency makes the PLL slow to lock up. Worse, though, it prevents suppression of the phase noise of the VCO around the loop. To avoid unacceptable intrinsic jitter, you must keep the loop filter's corner frequency high, or choose a VCO with low phase noise in the first place.

A good low-noise oscillator is a quartz VCXO. Because of their high-Q factor, however, you can't pull them far from their natural frequency, so they may have a pull range of only ±100 ppm, which may be insufficient for your requirements. On the other hand, a humble RC multivibrator VCO can have all the pull range you need but is essentially untuned, so it has large phase noise and is prey to all manner of interference. A few other VCO options exist between these extremes. To solve the pull-range problem with quartz, you could commission some VCXOs made of a special material with a lower Q, such as LGS (langasite) or lithium tantalate, which are expensive.

You could use a tuned-circuit LC VCO, which has a lower-Q factor than that of crystals, but at least it has a Q factor, so it can be designed with lower phase noise than a multivibrator. These circuits' wide range can cover both 44.1- and 48-kHz rates and can easily accommodate ±1000-ppm reference inaccuracy. Overall, this circuit is not a bad choice; if you're

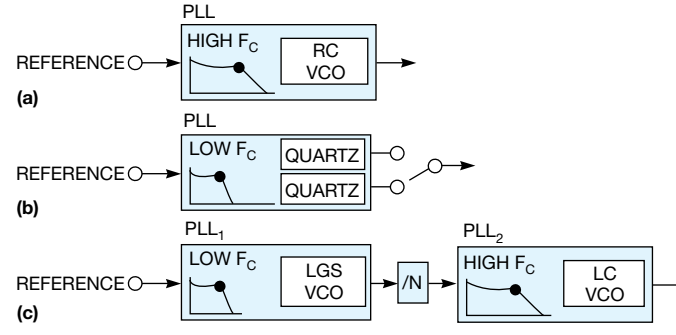

Figure 4 Three analog PLL examples are shown. A basic PLL chip operates in a digital-audio-interface receiver (a). A purpose-designed PLL provides converter-clock recovery, with a higher-Q VCO and a low loop-filter corner frequency (b). Two cascaded PLLs—the first, with an LGS VCXO for wide lock range and a low-corner-frequency filter, which rejects jitter, and the second, with a tuned-circuit VCO and a high loop-filter corner frequency to cover all sample-rate multiples—provide good intrinsic jitter (c).

picky, though, the intrinsic jitter won't be top-class if the corner frequency of the loop is dropped to where you'd like it.

In considering these trade-offs, it is helpful to look at some real-world examples of applying analog PLL technology to converter subsystems (**Figure 4**). The circuit in **Figure 4a** uses a basic PLL chip or, for an AES3 (Audio Engineering Society 3) or SPDIF (Sony/Philips-digital-interface) DAC, uses the PLL in the digital-audio-interface receiver. The VCO, however, has a low-Q factor and high phase noise, usually in the form of an RC multivibrator, which is vulnerable to all sorts of interference, especially power-rail and ground noise, and the corner frequency of the loop filter is high. These problems result in high intrinsic jitter and poor jitter rejection at audible frequencies.

The circuit in **Figure 4b** uses a purpose-designed PLL for converter-clock recovery, with a higher-Q VCO and a low loop-filter corner frequency. This setup results in good intrinsic jitter and jitter rejection, but the pull range may be insufficient, and you must carry the cost of two or more VCXOs.

The circuit in **Figure 4c** uses two cascaded PLLs—the first, with an LGS VCXO for wide lock range and a low corner-frequency filter, which rejects jitter, and the second, with a tuned-circuit VCO and a high loop-filter corner frequency to cover all sample-rate multiples. This circuit has no jitter so it requires no jitter rejection. If you make the LGS VCXO frequency 44.1 and 48 kHz, you can provide a sample-rate reference for the second PLL with a simple programmable divider. This approach has good intrinsic jitter and jitter rejection, works for all sample-rate multiples of 44.1 and 48 kHz, and has a wide lock range. Even with one VCXO, though, it's still expensive, and it still may have questionable performance at low comparison rates.

An even better approach is to adapt the dual-loop architecture as a hybrid PLL by implementing the first PLL in the digital domain, thus eliminating the trade-off of phase noise versus low corner frequency because the loop filter and the VCO are both entirely digital. The VCO—now an "NCO"—is jittery because it is a varying integer division of a fixed master clock, but inclusion of a sigma-delta modulator in the loop means that you can confine its jitter to high frequencies.

It is therefore straightforward to cascade the NCO's output into an analog PLL with a high corner frequency, which can then use an inexpensive VCO without intrinsic jitter. Furthermore, you can change the corner frequency in software to achieve fast lock and then extreme jitter rejection. The hybrid PLL is inexpensive because it requires no resonator-based VCO. Similar approaches are now available for audio use from a number of vendors, including Cirrus Logic (**Reference 4** and **Figure 5**). Some manufacturers even built them into data converters.

Another way to approach this problem is to use modern, low-cost SRC (sample-rate-converter) chips, which are achieving performance that can exceed that of the data converter itself. You might elect to operate the conversion element at a fixed rate provided by a local crystal, thus eliminating sampling jitter, and to convert the converter's input or output data rate. This approach can lead to other issues and places the responsibility on the SRC to achieve jitter rejection that matches the same standard as in the PLL model while also protecting the quality of your audio components.

POWER SUPPLIES

High-quality line-powered audio equipment has traditionally employed linear PSUs, but these devices have disadvantages of size, weight, heat, and cost and may need a manual line-voltage selector. Properly designed PSUs do have the advantage of not providing a source of high-frequency interference into the analog circuits. An SMPS eliminates these

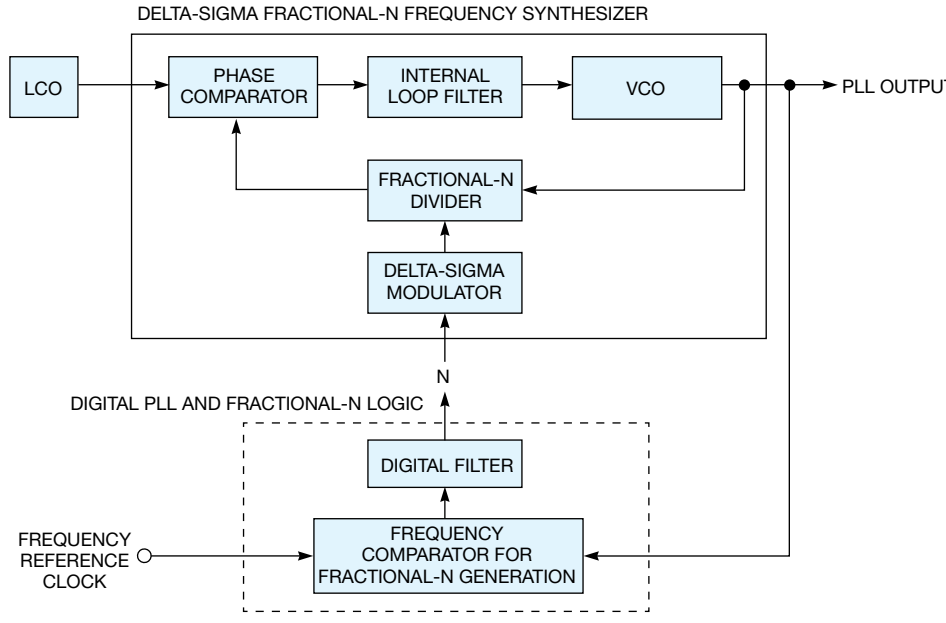

Figure 5 Cirrus Logic's C2000 hybrid PLL is inexpensive because it requires no resonator-based VCO.

disadvantages, but it must be carefully designed if it is not to become a major source of hostile switching noise. High-end-audio designers have traditionally shied away from using SMPSs.

You must design an SMPS in any type of equipment to meet the appropriate electromagnetic-compatibility standards for conducted and radiated emissions. Nowadays, this task is not difficult, with SMPS controller vendors providing application circuits that comply with these standards—usually, just meeting compliance requirements to save the costs of filter components. Unfortunately, the same sorts of misbehaviors that might cause an SMPS to be noncompliant can wreak havoc with audio performance, even at much lower levels. Thus, SMPS design for audio applications can be elaborate.

DRAWBACKS OF LOW-COST SMPSs

Converter systems often need a large number of power rails and may benefit from isolation between the digital and the analog parts, so a flyback architecture is a popular choice because it conveniently offers these benefits, which may also be useful in dc-powered situations. A variety of other simple SMPS architectures can be used instead; the problem for the uninitiated is generally how to choose among them.

In a flyback converter, dc—either directly input or rectified from the ac-line voltage—is switched through the primary of the flyback transformer by a transistor under the control of a device that regulates the duty cycle of a train of switching pulses to regulate the various secondary outputs. Rectified and filtered secondaries provide the power rails.

Figure 6 shows a flyback converter and its switching waveform. Stray capacitance, C_D, across the switch and the leakage inductance of inductor L_{LK} causes the high-frequency oscillation at the point at which the switch turns off. This oscillation is a largely unavoidable source of hostile RF. You can control its amplitude with snubbers to protect the switch, but this approach can make the interference even worse. The low-frequency oscillation before the switch turns on is a consequence of the stray capacitance and the primary inductance, L_p. The switch interrupts the oscillation at a random voltage, causing potential interference from the large switching voltage and current.

The main problem, then, with the basic flyback topology—and with most other basic topologies—is that the transistor switches hard and randomly, causing high levels of radiated and conducted interference to invade the analog audio parts. You are now on a slippery slope, and can't do much to reduce the source of the problem. You can keep the switching loops as small as possible to reduce radiation, you can optimize the ground topology and make critical tracks wider to reduce ground noise, and you can tame the edge times with snubbers, but only at the cost of reduced efficiency and increased heat. So you end up having to take disproportionate steps in the vulnerable parts to make sure that the audio remains clean. These steps can include the use of screening cans, split grounds, or galvanic isolation.

Another problem is the random frequency of the SMPS controller, which can produce interference at the beat frequency between itself and, for example, the audio sample rate, thus making it impossible to confine it to some inconspicuous part of the spectrum. A possible approach is to lock the switching frequency to some multiple of the sample rate to remove the beat frequency, but this approach can be problematic. The regulatory variation of the duty cycle can cause its own beat, and some types of SMPS controllers vary the switching frequency to effect regulation. You could even introduce a situation in which a software bug or a wayward sample rate could collapse the power rails. It's easy to see why designers are reluctant to use SMPSs in high-performance audio equipment, but they often have no choice in dc-powered situations, and SMPSs are small and inexpensive.

RESONANT AND QUASIRESONANT SMPSs

Ideally, to combine the benefits of a linear supply and an SMPS, you would like to find a way of passing a high-frequen-

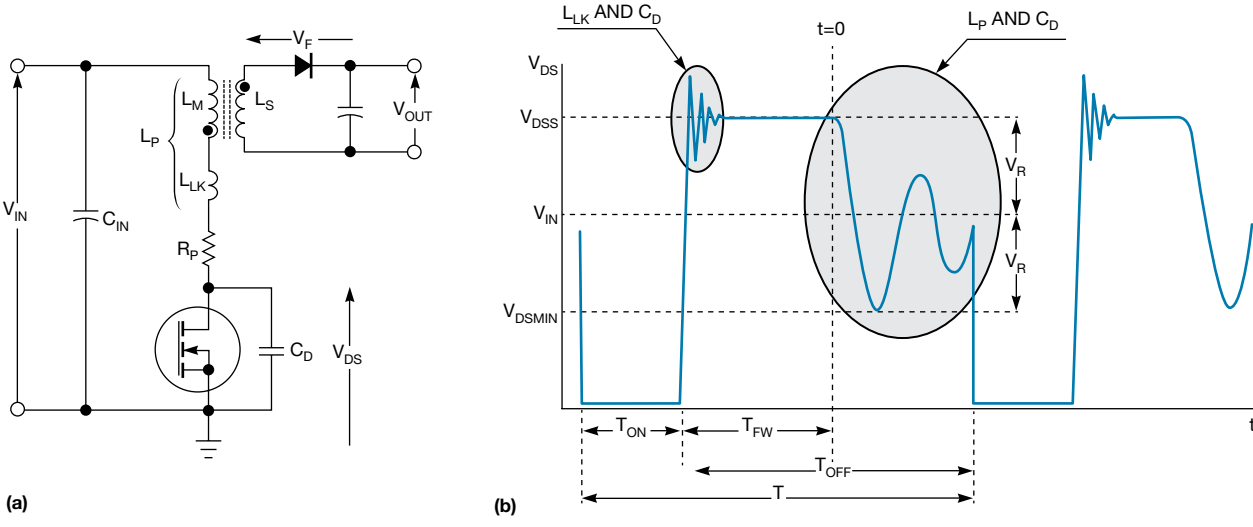

Figure 6 In a flyback converter (a) and its switching waveform (b), stray capacitance, C_D, across the switch and the leakage inductance of inductor L_{LK} causes the high-frequency oscillation at the point at which the switch turns off.

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cy sine wave through the transformer. An approximation to such an approach is a resonant SMPS. To losslessly achieve this architecture, it is usual to generate the sine wave by placing a resonant LC-tank circuit in the primary; a neat trick is to use the primary inductance as the inductor. The stimulus for the waveform is still a hard-switching transistor under clever control, but the resonant circuit tunes the primary waveform to an approximation of a simple sine wave, with the switching happening at 0V or 0A moments, all of which leads to less hostile switching noise.

On the other hand, resonant designs tend to be somewhat more costly and larger than flyback designs. A major drawback with many resonant architectures is that you must tailor the LC-tank circuit to the switching frequency and dc input voltage to maintain resonant and zero-switching operation, which makes offline universal input design problematic unless you incorporate power-factor correction.

A good compromise is a quasiresonant converter. The idea here is that, because the problems in a simple flyback converter happen only at the moments of switching, it is necessary to find a way of creating a resonant waveform only at the switching points. You can achieve this goal by simply introducing primary resonance into an ordinary flyback topology and making the controller clever about deciding when to switch. **Figure 7** shows a zero-voltage-switching, or valley-switching, quasiresonant converter, which is a low-cost way to cut SMPS emissions at their source (**Reference 5**).

In this case, you create the tank circuit by simply adding a large capacitor across the switch. The tank circuit slows the switch-off rise time, and the controller arranges the switch-on instant to coincide with a valley in the low-frequency oscillation; this approach inherently makes the cycle period variable with an attendant spread-spectrum effect, which can improve interference and which increases EMC margins (**Figure 8** and **Reference 6**).

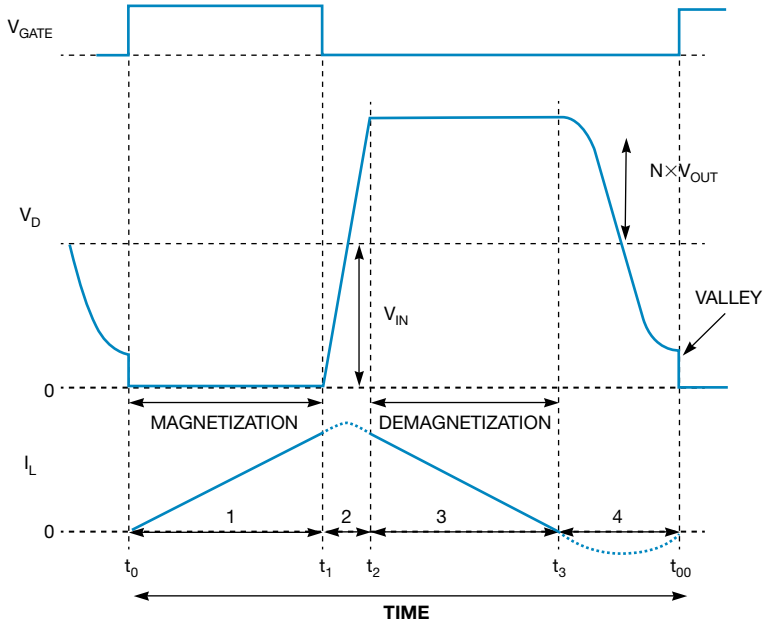

Figure 7 A zero-voltage-switching, or valley-switching, quasiresonant converter is a low-cost way to cut SMPS emissions at their source.

SMPS SELECTION

It is often difficult for the uninitiated to make the correct choice of SMPS architecture for audio because most SMPS-controller vendors organize their selection tables by power capability. They assume that audio designers, like other designers, will want to choose the cheapest approach for their power requirement. The recommended SMPS for low-power applications such as this one—say, less than 20W—is usually a basic, hard-switching type because the power is low enough for its emissions to remain below statutory EMC limits with minimal filtering and for the losses resulting from its indiscriminate switching to be insufficient to set it on fire.

Higher-power applications in which you must control switching noises and losses require the use of resonant and quasiresonant topologies. For audio, however, it's often a good idea to make a low-power implementation of a high-power topology in the interest of achieving minimum emissions; you can usually make up for the extra cost by not having to armor-plate the audio parts.

OTHER CONSIDERATIONS

Cross-regulation—varying load conditions on individual rails—can cause the voltages of other rails to vary and is often a problem with multirail-SMPS designs because the regulatory mechanism of the controller can generally operate on only one rail. In performance-critical applications, it may be necessary to provide linear postregulation on analog-power rails from the SMPS. If so, take care to provide adequate cooling for the linear regulators. Linear regulators can usually regulate over only a limited frequency range, and the switching products from the SMPS can easily exceed this range, causing them to pass straight through the regulator. It is therefore a good idea to use ferrite beads ahead of linear postregulators.

Line-powered linear and SMPS equipment usually draws current from the mains only during voltage peaks, which can cause distortion to the power line, with possible detriment to the performance of other sensitive audio equipment. It may be beneficial to incorporate PFC into your SMPS design to cause the least possible distortion to the power waveform. You can be sure, however, that all the other equipment around the SMPS will probably be causing distortion anyway. Some PFC schemes allow tight control of the rectified voltage ahead of the SMPS, which can allow you to further reduce switching noise in resonant and quasiresonant designs by ensuring no switching for any input voltage.

As well as applicable safety, EMC, and disposal legislation, line-powered equipment is subject to or will become subject to various territorial legislation for standby-power consumption, when applicable, and operating efficiency—for example, under the European Union's Ecodesign Directive and the voluntary US EnergyStar program. Although territorial legislations vary,

maximum standby-power consumption of 0.5W and minimum operating efficiency of approximately 80% are typical for a 20W device.

ANALOG-SIGNAL PATH

Analog performance is the limiting factor in many converter designs. Somewhere along the line, perhaps you forgot some of this wisdom. All of the buffer amplifiers, gain stages, and other components between the outside world and the ADC and between the DAC and the outside world are obvious areas in which good design practice will pay dividends. It is no mean feat to maintain the performance of a flagship data converter through the analog circuits, particularly if you must incorporate significantly high performance.

In general, use a ground plane for analog circuits and take advantage of the small surface-mount-technology packages that are now available. Lay things down instead of standing them up. These measures are free and will reduce susceptibility to interference and crosstalk.

Of particular importance are the buffer circuits, which drive by the input of the ADC or are driven by the output of the DAC. In general, the safest policy is to stick with the exact circuit topology and components that the converter manufacturer recommends. The vendor will have spent a long time coaxing the best out of the device by tweaking its buffer. However, this scenario is not always true. With experience and care, it is sometimes possible to exceed the application-note performance. On the other hand, if cost is important, you can often scrimp a bit on op-amp types.

Sigma-delta ADC inputs often have a nonlinear-input characteristic and produce aliasing components if subject to high frequency, so an ideal ADC buffer must achieve a lot of high-frequency roll-off—but without compromising in-band flatness—and a low output impedance. It's better to avoid the passive pole between the output of the buffer and the input of the converter and to instead use, for example, an analog-input buffer (**Reference 7**).

Many high-quality DACs have current outputs, requiring an outboard current-to-voltage-converter circuit. Sigma-delta DACs often produce significant out-of-band noise, and the IVC must filter, cancel, or both filter and cancel this noise in the first instance. Therefore, to maintain in-band linearity, the IVC must behave linearly at frequencies well above the audio band. If you are tempted to stray from the manufacturer's recommended IVC design, bear in mind the bandwidth requirement and note that the data converter's output loading will probably have to be similar to that of the application circuit for optimum performance.

As for the rest of the analog-signal path, it is important to choose the right components and circuit topologies. The most straightforward way is to use op amps. This approach is currently a good policy except in a few situations, such as microphone/phonograph preamps and high-current outputs. It will pay to familiarize yourself with the noise models for op-amp circuits, such as those that **Reference 8** describes, and to implement a spreadsheet to calculate noise levels for your circuit. A simpler but less versatile approach is to use op-amp manufacturers' noise-reckoning tools (**Reference 9**). The best approach is to use a full-blown Spice simulator (**Reference 10**).

You will find that your choice of op amps in each stage is generally restricted to relatively few that have the requisite voltage-noise, current-noise, or both voltage- and current-noise performance. The world is full of op amps, most of which are not good for audio. On the other hand, beware the best-audio-op-amp syndrome.

No op amp will behave best in every audio stage. In each case, you must select the right one for the job. Usually, you can make this selection from looking at available data or by trading off requirements against cost, power, and other factors. But don't be afraid to use trial and error in the end, although doing so requires some determination and good eyesight in this age of SMT. With some dexterity, you can persuade dual-inline sockets onto the SOIC sites in your prototype. In general, it's a good idea to use dual-op-amp sites because doing so is a good trade-off of cost and choice and allows tight layout in balanced circuits.

Designers generally prefer inverting-op-amp topologies over noninverting models because the inverting devices' input terminals operate at virtual earth. The dynamic input-common-mode voltage of noninverting configurations

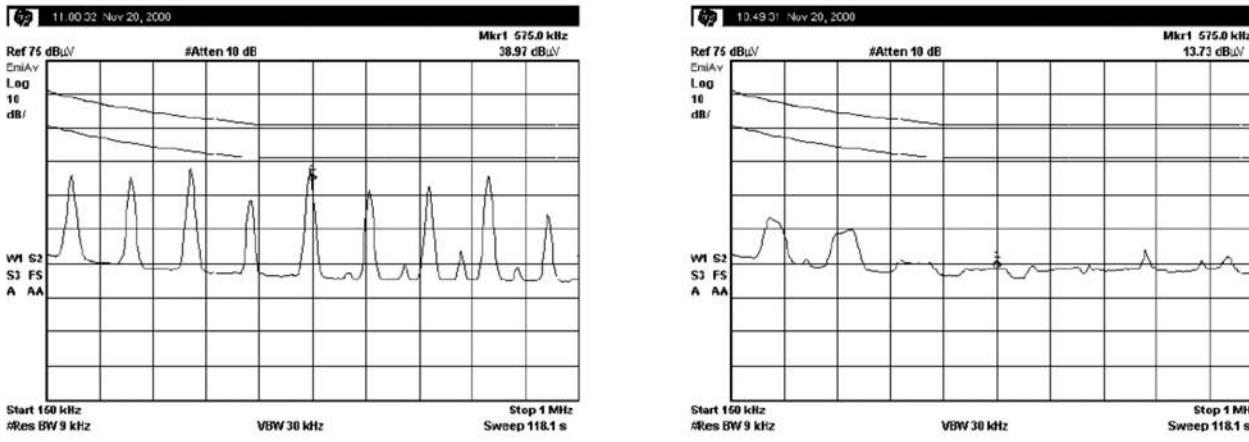

Figure 8 The tank circuit slows the switch-off rise time (a), and the controller arranges the switch-on instant to coincide with a valley in the low-frequency oscillation (b).

may add distortion, particularly at high frequencies with some op amps. Consider adopting a fully balanced topology end to end—perhaps using a "symmetrizer" in the ADC's case to achieve balance through the channel even with unbalanced inputs. Avoid mode-conversion types, however. Using a fully balanced topology not only reduces interference and crosstalk but also can achieve higher performance because distortion mechanisms often tend to cancel. Most high-end data converters operate in a balanced mode anyway.

It is important to select a gain structure that maximizes the dynamic range, or SNR, and thus minimizes the need for excessively low-noise design, with its attendant cost. Even so, resistor values must be low enough for their thermal noise to be out of the picture but not low enough to bring problems of overdissipation or circuit loading.

The linearity of resistors and capacitors is also important. Resistors must be metal-film or thin-film types, not the usual chip resistors, which change resistance according to voltage and the seasons. Capacitors must be low-k ceramic types, such as C0G and NP0 types, or low-loss plastic, such as polystyrene. Failure to observe these rules leads to nonlinearity and distortion in most circuit topologies. Keep electrolytics out of the signal path; there are other ways to ensure extended low-frequency response.

PCB layout of the channel circuits is critical for minimizing both interference and interchannel crosstalk. Make sure that the op amp's output and the ground nodes of the stages are outermost and that the op amp's input nodes are innermost in your channel-strip layout.

Pay attention to the bandwidth of your stages. It's not always better to go for a dc-to-light approach. Limiting the bandwidth at the top end reduces susceptibility to interference, and the presence of excessive high frequency, even if inaudible, does no good to the in-band signal. Limiting the bandwidth at the bottom end removes wandering dc, which can cause problems with mixing and switching, as well as the risk of unexpected overload. On the other hand, keep a healthy disrespect for the –3-dB, 20- to 20-kHz approach. Extend the top and the bottom end beyond the bare essentials when possible and strive to keep the area between flat; you will notice the difference.

REFERENCE VOLTAGE

Nearly all data converters have at least one accessible reference-voltage pin, reference-current pin, or both. The reference multiplies the input to the converter to produce the output, so how you handle the reference is just as important as the analog-signal path. Any noise or interference on the reference modulates the converter's output. You must filter internally generated voltage references by placing suitable capacitors close to the pins. This approach usually requires an assortment of low-value, high-frequency, large electrolytic or tantalum capacitors.

In some cases, you may want to drive a voltage reference externally from a well-regulated and filtered source. Some converter devices require both high and low reference voltages to define their operating range, and some require separate references per channel. Although users can sometimes to some degree modify the reference voltages, manufacturers often optimize converter performance at a particular voltage, and it's best to stick with that voltage. When your design has distortion or noise problems, remember to look at the reference. If modulation issues, such as sidebands or noise skirts around the signal frequency, get worse with increasing signal frequency, it's jitter. If those issues don't get worse, then the problem is most likely the reference voltage (**Reference 11**).

DIGITAL PARTS

Any low-quality digital processing in the signal path can undo all of your good work in the analog domain. Make sure that your design has enough precision everywhere and that algorithms are beyond reproach. Culprits often include dithering, noise-shaping, and dynamics processing. Remember, too, those parts of the digital-signal path that designers often overlook. For computer interfaces, the driver or parts of the operating system that you thought you had bypassed sometimes let you down. You must be able to test your entire signal path, so make

sure that your dual-domain audio-test equipment can work in the computer domain, directly interfacing with your driver layers.

In the old days, it was almost possible to keep all of the digital parts of a converter system ticking at some multiple of the sample rate. Consider the simple case of an AES3-interfaced converter with no DSP and no microcontroller. Nowadays, though, you must have a boxload of computers, including DSPs, RISC processors, and FPGAs, all running asynchronously, and probably a computer interface buzzing away across the entire spectrum. Although lower operating power, lower core voltages, and smaller dice and packages contribute to reducing the hostile intent of digital electronics, a designer can do little to fix it beyond observing good EMC design at ports and good power decoupling and filtering.

You must make some fundamental decisions at the outset of your design. These decisions include the choice between line power and dc power, as well as choices regarding whether you can put your design into its own metal box, whether it must cohabit with digital parts, or whether it must reside in a host computer. You also must decide whether you need and whether you can afford screening cans. Another decision comes up when you consider construction: Can you use a multilayer PCB with groundplanes, a small SMT device, or another configuration? What about isolation? Can you galvanically isolate the analog and digital domains using optical or magnetic isolators? This isolation can be beneficial in computer or computer-interface cases, in which the digital ground can be toxic. You also need to weigh EMC compliance and efficiency. Project requirements and component budget probably dictate the answers to these questions.

The objective assessment of converter systems, both during design and in general, is a complex subject and the subject of many international standards, such as IEC 61606-3 and AES17-1998 (**references 12**, **13**, and **14**). It is useful, however, in many situations to make a simpler assessment. For many engineers, this assessment involves instead using listening tests to determine audibility. The debate about whether measuring or listening is better will rage forever. However, developing high-performance audio requires both methods. Some engineers believe that it is better to use measurement to debug the design and to worry about listening tests after that.

For debugging, first equip yourself with an audio analyzer, which can stimulate and measure in the analog, digital, and computer domains. Analyzers should be able to display a continuous high-resolution FFT, and they should be user-programmable so that you can automatically hop among key measurements. You must be able to define all of the key measurement parameters when you set up the debugger. Make a lead to connect a pair of small probes to the analog analyzer's input so that you can measure between all the stages. SMPS and computer-based devices also need a means of seeing the wideband spectrum, which EMC precompliance also requires. **Table 1**, available with the Web version of this article at http://bit.ly/w29NCL, provides a guide to the most important audio-performance parameters that apply to conversion systems. EDN

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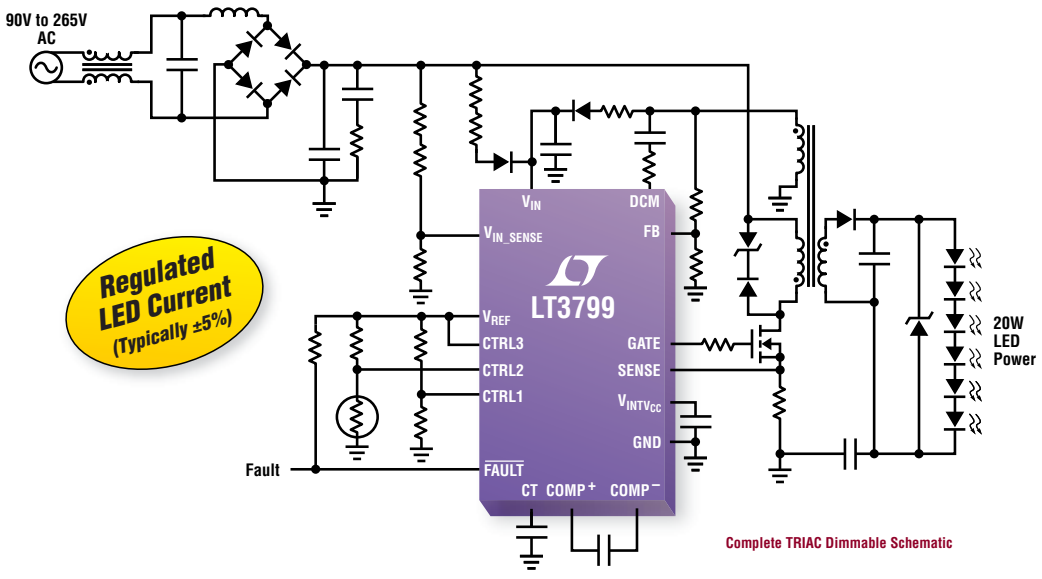
AUTHOR'S BIOGRAPHY

Ian Dennis is technical director of the Prism Sound Group, a manufacturer of audio converters, test-and-measurement equipment, audio workstations, and media servers. He has been designing audio equipment since the early 1980s. At Prism Sound, he focuses on R&D and production activities but also works on a few design projects now and then. Current interests include audio conversion, audio-test equipment and methods, media-streaming devices, and audio networking. Dennis is vice chairman of the Audio Engineering Society SC-02-01 Standards Committee for audio test and measurement and also works on standards development within the BSi and International Electrotechnical Commission, most recently contributing to IEC 61606-3 test methods for professional digital-audio equipment and ITU BS.1770 loudness metering.

Isolated LED Current Control with Active PFC



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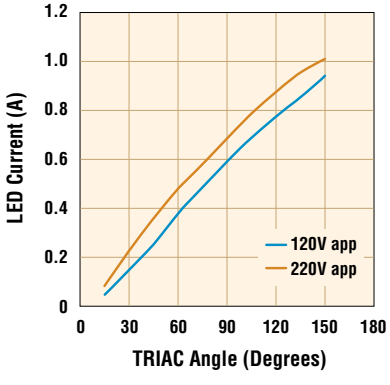
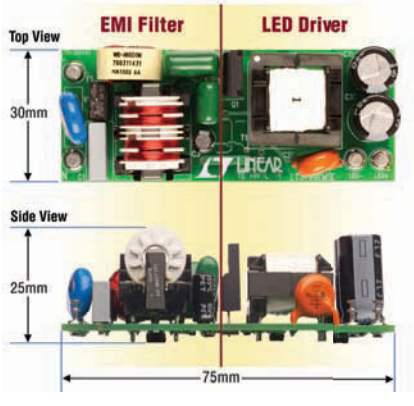
LED Current vs TRIAC Angle



LT3799 Demo Board (25W)



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LINEAR TECHNOLOGY

CMOS gate makes long-duration timers using RC components

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

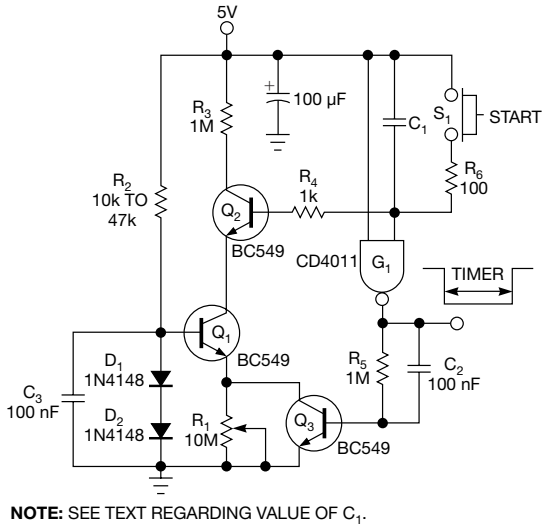
The CD4011 CMOS NAND gate has a typical input current of 10 pA at room temperature. You can charge a capacitor connected to the gate input with currents on the order of hundreds of picoamperes and neglect the influence of the gate-input current on the charging time of the capacitor. You normally need large-value resistors to limit currents to this low level. These resistors are not commonly available. You can instead use a transistor as a current attenuator, despite its more usual amplifying nature.

The circuit in **Figure 1** uses one CD4011 package containing four NAND gates, which you can use to build four independent long-duration timers. Note, however, that temperature variations and component parameters affect the timing, a situation that may be acceptable if you are not concerned about accurate timing and need only a simple circuit without large-value electrolytic capacitors and resistors.

The series-connected diode voltage drops of D_1 and D_2 bias current source Q_1. The resulting voltage across R_1 is a Q_1 base-to-emitter-voltage junction drop less and sets the Q_1 collector current, which is also the Q_2 emitter current. The resulting Q_2 base current is its emitter current divided by its current gain and charges timing capacitor C_1.

Before the start of the timed period, the gate output is high, biasing on Q_3 and Q_1, allowing C_1 to charge through the base-emitter junction of Q_2. This action holds the gate input sufficiently below its switching threshold to maintain its high output state. Momentarily closing and then releasing S_1 starts the timed period by discharging C_1. This action drives the gate output low and ensures that Q_3 is biased off, which allows Q_1 and Q_2 to slowly charge C_1 through the constant-current action. The power-supply current draw of the gate increases somewhat as its input voltage pulls away from the 5V rail.

When the C_1 charge reaches the gate-switching threshold of approximately 2.5V, the gate output begins to rise, turning on Q_3. This action increases the current through Q_1 and Q_2, resulting in saturation of Q_2 and a faster charging of C_1. This positive feedback provides the necessary hysteresis to complete the charging of C_1 and return the gate output high.



NOTE: SEE TEXT REGARDING VALUE OF C_1.

Figure 1 A constant-current source and current divider reduce the timing capacitor current to a low level to increase the charging time.

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Linearity with changes in R_1 is impossible due to variations in the transistor's current gain. The built and tested circuit does exhibit linearity with the value of timing capacitor C_1, which you can choose experimentally for the required time. Once you determine a time for a short interval, such as that for a 10- or a 100-nF capacitor, you can use this knowledge to scale to longer timing. In the tested circuit, with R_1 set to 1 MΩ, a C_1 value of 10 nF results in a time of 10 sec; a C_1 value of 100 nF increases the time to 100 sec.

Editor's notes: Constructing a low-current circuit is challenging. Some types of PCB-soldering flux can become conductive, wreaking havoc with what should be a tiny current. Consider "open-air" connection of the Q_1-emitter collector and the Q_2-emitter base leads to remove them from the board.

Transistor-leakage currents and current gains vary widely from device to device and with temperature. This variation can drastically affect the expected low-level current and capacitor charge time. Although the CD4011's typical input current

is 10 pA at room temperature, it could be as high as 100 nA and increase to 1 µA at high temperature. Likewise, the transistor collector-to-base leakage could be a maximum of 15 nA at room temperature and 125 µA at high temperature, and it approximately doubles for every 10°C rise in temperature. It might be necessary to hand-select transistors and CD4011 inputs or devices to overcome this problem. Also, remember to tie any other unused CD4011-gate inputs to ground or 5V to avoid floating-input problems.

Do not set R_1 so low that Q_1 or Q_2 saturates during the timed period; they must remain in their linear region as set by the value of the Q_2 collector resistor.

Timing capacitor C_1 should have a high-quality, low-leakage dielectric, such as polyester; check the leakage specifications of the size and type you intend to use for suitability with the low-level current. EDN

Microcontroller drives piezoelectric buzzer at high voltage

Mehmet Efe Ozbek, PhD, Atilim University, Ankara, Turkey

Piezoelectric buzzers find wide use in embedded systems for audible-signal generation. You can drive a piezoelectric element directly from a microcontroller's I/O pins, but the maximum voltage rating and loudness of a piezoelectric buzzer are typically several times larger than the voltage an I/O pin supplies. Using four enhancement-mode MOSFETs that connect in an H-bridge configuration, the microcontroller can drive the buzzer at a high alternating voltage. The gate terminals of the N-channel transistors in the lower arms of the bridge can connect directly to the microcontroller's I/O pins. The voltage level on the I/O pins is insufficient for switching the P-channel transistors, however.

The circuit in **Figure 1** solves the problem using a cross-coupled configuration. The operation is as follows: The microcontroller turns Q_2 on and Q_4 off by applying high- and low-logic-level voltages to I/O Pin 1 and I/O Pin 2, respectively. The voltage on Node A goes low, turning on Q_3. Node B is now 15V, which is sufficient to keep Q_1 off. The voltage on the piezoelectric buzzer is 15V. The microcontroller then toggles I/O Pin 1 and I/O Pin 2, resulting in a piezoelectric voltage of –15V for an effective 30V p-p. These cycles are repeated to generate an alternating voltage with the desired frequency. By using MOSFETs with proper voltage ratings, you can use higher supply voltages that the piezoelectric element can tolerate. EDN

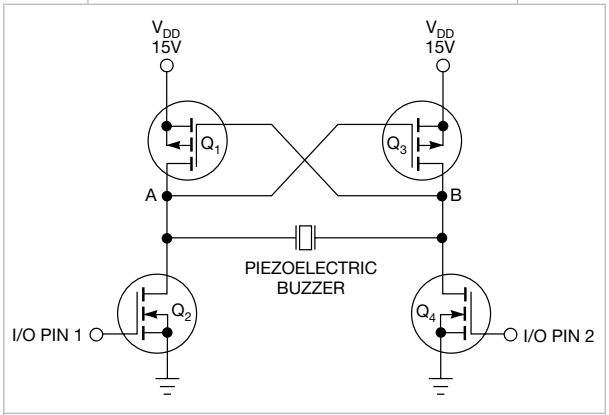

Figure 1 This cross-coupled configuration enables you to drive a piezoelectric buzzer from a microcontroller's I/O pins.

Circuit simultaneously delivers square and square root of two input voltages

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

This Design Idea requires inputs from the circuit in a previous Design Idea (**Reference 1**). IC_1 and IC_3 are ADG5213 quad switches with individual logic-level control inputs (**Figure 1** and **Reference 2**). With a high input, switches S_2 and S_3 are open, and switches S_1 and S_4 are closed. The switches toggle to opposite states with their control inputs low. The circuit is in the idle pretriggered condition. During the initial idle condition before a clock rising-edge trigger, Q is high and, through IC_8, holds switches S_2 and S_3 of IC_1 in the open position.

$\overline{Q}$ is low, and, through IC_7's Reset high closes IC_1's S_1 and S_4, discharging C_{T2} and C_{T4} and zeroing the input voltage to unity-gain amplifiers IC_{2D} and IC_{2C}. $\overline{Q}$ low also sets Track 2 low through IC_6 and holds IC_3's S_1 and S_4 in the open position. The circuit retains any sampled voltages from a previous operation in sample-and-hold capacitors C_{S1} and C_{S2}; these voltages appear at V_{OUTX} and V_{OUTY} through unity-gain amplifiers IC_{2A} and IC_{2B}.

Signals V_{OUTL} and V_{OUTQ} from the linear and quadratic pulse generator are at 0V during idle, holding comparator outputs IC_4 and IC_5 low. A rising trigger edge at the clock signal begins the ramp generation of V_{OUTL} and V_{OUTQ}. The Q and IC_8 outputs fall low, closing IC_1's S_2 and S_3 and ensuring that Track 2 remains low. $\overline{Q}$ rises and forces Reset low through IC_7, opening S_1 and S_4 of IC_1 and allowing C_{T2} to follow the rising V_{OUTQ} and C_{T4} to follow the rising V_{OUTL}.

When linear ramp V_{OUTL} rises to

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analog input V_X, IC_4's output rises and, through IC_8, Track 1L opens S_2 of IC_1 and allows C_{T2} to hold the present level of V_{OUTQ}. In a similar manner, when quadratic ramp V_{OUTQ} rises to analog input V_Y, IC_5's output rises and, through IC_8, Track 1Q opens IC_1's S_3 and allows C_{T4} to hold V_{OUTL}'s present level. The pulse generator terminates when the ramps reach 5V. The ramps then fall back to 0V, Q returns high, and $\overline{Q}$ returns low.

The rise of Q immediately triggers IC_6 to generate a high pulse of approximately 20 µsec on Track 2 based on R_{D1} and C_{D1}. This action closes IC_3's S_1 and S_4, allowing the sampled voltages on C_{T2} and C_{T4} to transfer to C_{S1} and C_{S2} through unity-gain amplifiers IC_{2D} and IC_{2C}. Unity-gain amplifiers IC_{2A} and IC_{2B} present the C_{S1} and C_{S2} voltages at V_{OUTX} and V_{OUTY}. When Track 2 returns low, IC_3's S_1 and S_4 open, and the sampled voltages on C_{S1} and C_{S2} are retained.

The fall of $\overline{Q}$ triggers IC_7 to produce a 50-µsec delayed rise on Reset, which R_{D2} and C_{D2} time to occur after Track 2 has returned low and the sampled voltages are safely captured on C_{S1} and C_{S2}. Reset's high state closes IC_1's S_1 and S_4, discharging C_{T2} and C_{T4} in preparation for the next trigger. V_{OUTX} is the squared voltage of input V_X, and V_{OUTY} is the square root of the voltage of input V_Y. You can view the equations at www.edn.com/120301dia. EDN

REFERENCES

1 Štofka, Marián, "Positive edges trigger parabolic timebase generator," *EDN*, July 28, 2011, pg 51, http://bit.ly/yYvu3F.

2 "ADG5212/ADG5213 High Voltage Latch-up Proof, Quad SPST Switches," Analog Devices, 2011, http://bit.ly/w6XTO3.

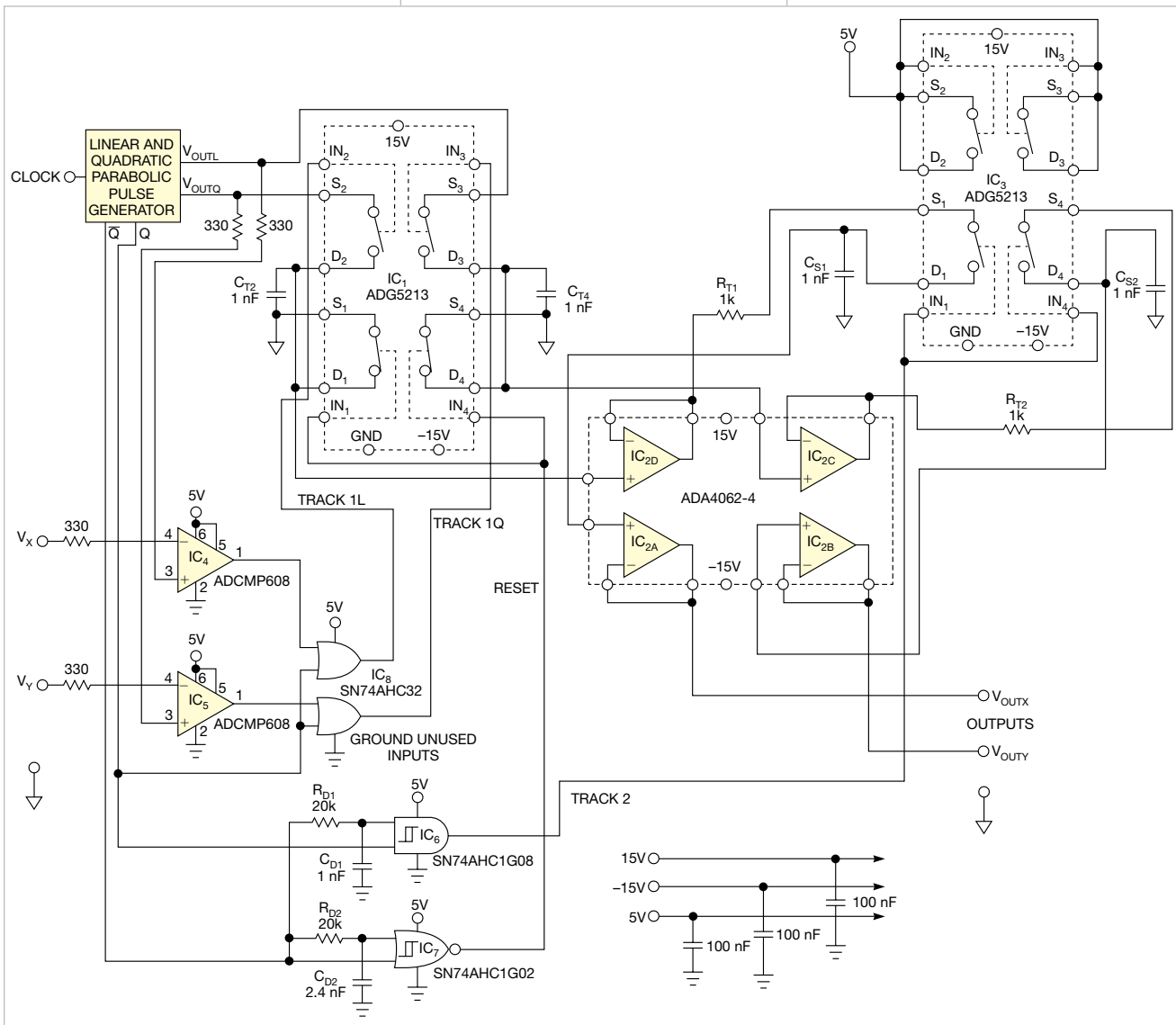

Figure 1 With this circuit, you can find the square at Channel X and the square root at Channel Y for any positive dc or slowly varying voltages of 0 to 5V.

designideas CLASSICS

Originally published in the April 5, 1979, issue of *EDN*

Conversion circuit handles binary or BCD

R Srinivasan, R Ramesh, and DK Murthi,
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Systems requiring arithmetic operations on data usually perform those operations in binary form. As a result, they must convert the data to BCD form for display purposes. Address-selection information from digit switches, on the other hand, must be converted to binary form for use in memory-addressing operations.

For applications not requiring fast conversion, a single circuit that can perform both conversions proves adequate. One such circuit (**Figure 1**) utilizes up/down counters to obtain the desired results. To perform binary-to-BCD conversion, preset the binary value in the binary counter and clear the BCD counter. The binary counter counts down while the BCD counter counts up, and when the binary counter reaches zero, the BCD counter holds. For BCD-to-binary operation, the BCD counter counts down from the BCD value while the binary counter counts up. EDN

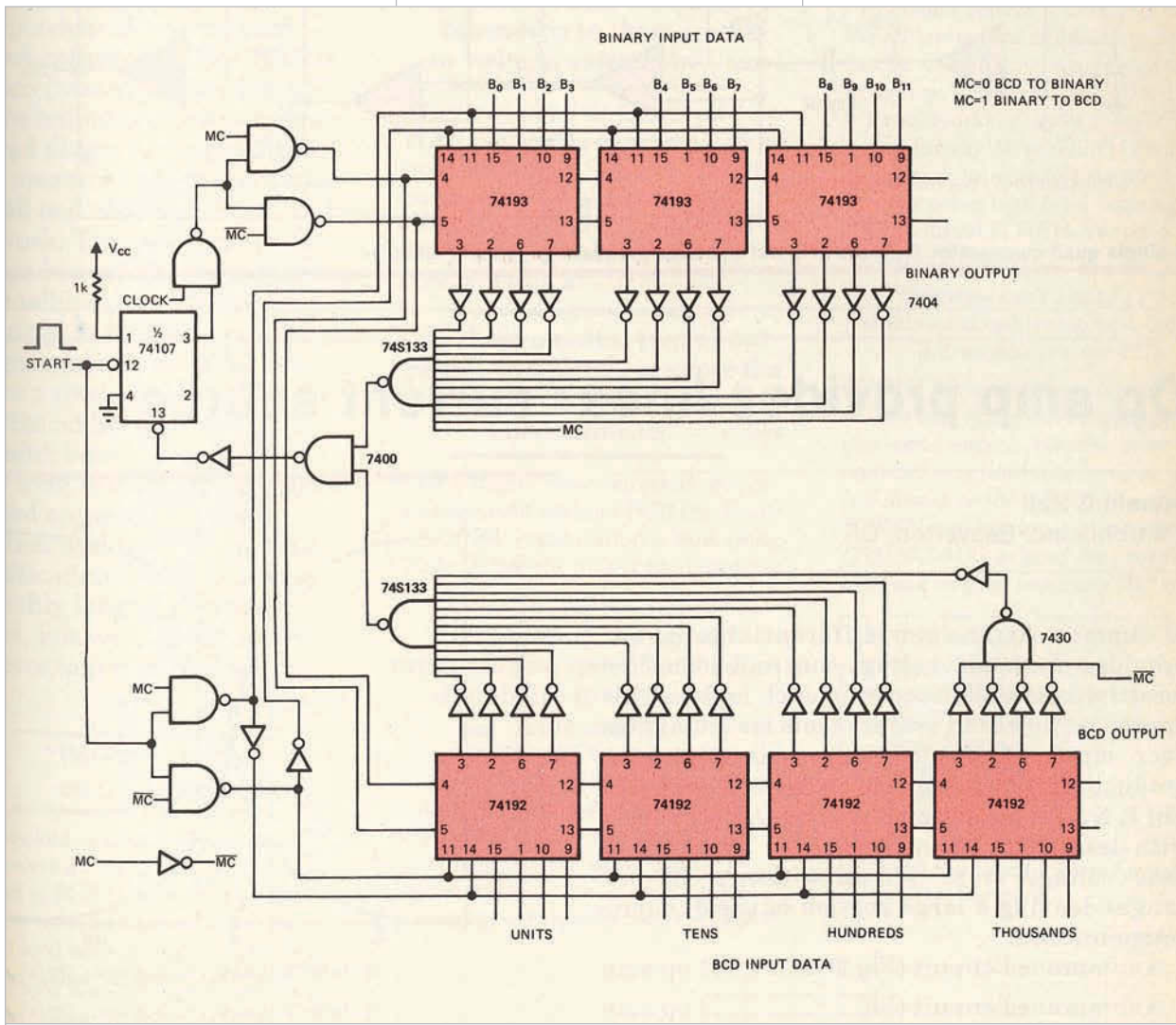
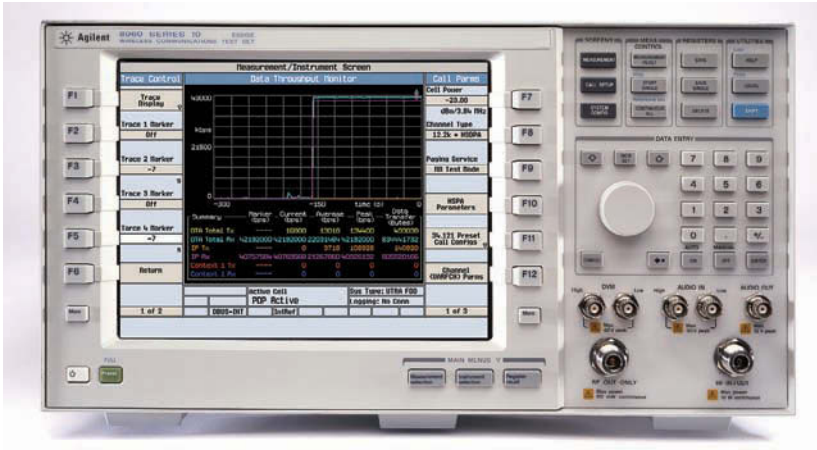


Figure 1 Separate binary and BCD up/down counters permit both binary-to-BCD and BCD-to-binary conversion in one circuit.

productroundup

TEST AND MEASUREMENT



Agilent E5515E wireless-communication test set accelerates design

The E5515E 8960 series 10 wireless-communication test set supports GSM, GPRS, EGPRS, E-EDGE, WCDMA, CDMA2000, 1×EVDO, EHRPD, TDSCDMA, TDHSDPA, TDHSUPA, IS-95, TIA/EIA-136, and AMPS wireless-device testing. The device has a 292- to 2700-MHz frequency range, including all commercial 3GPP and 3GPP2 frequency bands. Other features include a –110 to –13-dBm output-level range with modulation, a VSWR of less than 1.2-to-1 at 400 to 2000 MHz, and less than ±1-dB channel-power measurement accuracy. The Agilent E5515E mainframe is priced at $59,200, including all hardware options; software options are available at additional cost.

Agilent Technologies, www.agilent.com

Planar Caban R54 vector reflectometer measures S_{11} parameters

The Caban R54 vector reflectometer measures S_{11} parameters over an 85-MHz to 4.2-GHz frequency range. The device measures magnitude and phase of reflection coefficient, cable loss, and distance to fault. Per-point measurement time is 200 µsec, and frequency-setting resolution is as high as 10 Hz. The USB-powered device measures 117×39×19 mm, weighs 0.25 kg, and sells for $2995.

Planar LLC, www.planar.chel.ru

Aaronia spectrum analyzer offers real-time data streaming

Aaronia's Spectran V5 series of spectrum analyzers, scheduled to start shipping in 2012, offers extremely low-noise signal processing—up to 170 dBm/Hz—as well as a 200-MHz real-time bandwidth. Each spectrum analyzer provides real-time streaming and a real-time remote control for GSM, WLAN, and USB and has a TFT display with 800×480-pixel resolution. The analyzer utilizes an integrated 3-D motion sensor and a 3-D magnetic-field sensor. It uses 480-kbps USB 2.0 and has a USB slave interface to connect devices such as GSM, WLAN, printer, and memory. A micro-SD slot supports SDHC cards with more than 10 Mbytes/sec, and an integrated lithium-polymer battery with 8000 or 16,000 mAhr provides as much as three or six hours of runtime, respectively. The analyzer features modular construction for fast extension and customization of the front end and also includes a directional-tracking and EMC antenna, an aluminum carrying case, a battery charger, a power supply, and an international adapter set. The included MCS real-time spectrum-analyzer software runs with any operating system, including Mac OS, Linux, and Windows, and provides real-time remote control with any of the vendor's Spectran spectrum analyzers. Pricing starts at €2998 (approximately $3950) for the 10-MHz to 2.5-GHz Spectran HF-8025 V5.

Aaronia AG, www.aaronia.com

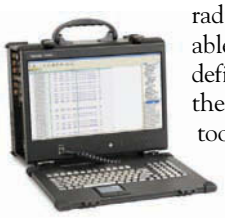
Pico 4262 scope includes arbitrary-waveform generator

The two-channel, 16-bit PicoScope 4262 has a built-in low-distortion signal generator. With a 5-MHz bandwidth, it can analyze audio, ultrasonic, and vibration signals; characterize noise in switched-mode power supplies; measure distortion; and perform precision-measurement tasks. The scope includes a function generator and an arbitrary-waveform generator that has a sweep function to enable frequency-response analysis. It also offers mask-limit testing, math and reference channels, advanced triggering, serial decoding, automatic measurements, and a color-persistance display. In spectrum-analyzer mode, the scope provides a menu of 11 automatic frequency-domain measurements, such as IMD, THD, SFDR, and SNR. The PicoScope 4262 connects to any Windows XP, Vista, or Windows 7

computer with a USB 2.0 port. The unit sells for £750 (approximately $1200).
Pico Technology, www.picotech.com

Tektronix TPI4000 analyzer lets users test multiple serial protocols

The TPI4000 protocol-analyzer series allows users to perform multiple test functions and to look at a variety of protocols, such as Ethernet, Fibre Channel, and common public-radio interface. A user-editable database allows users to define custom protocols using the optional protocol-editor tool. The series includes the portable TPI4202, which has a built-in monitor and keyboard and supports as many as eight ports, and the 4U-rack-mount TPI4208, which supports as many as 32 ports. Pricing for a complete system starts at $40,000.
Tektronix, www.tektronix.com



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Rigol Technologies Inc, www.rigolna.com

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DAN DULL • NOVO ENGINEERING

Printer parking brake

About 15 years ago, I was working for a wide-format-ink-jet-printer company in the San Diego area. The printers we designed could print on rolls of paper that were 5 feet wide and several hundred feet long. Needless to say, we needed to send an enormous amount of data to these printers to keep the print heads moving and the paper advancing. One of the key product requirements was throughput, specified in square feet per hour. Ideally, the print head's firing rate governed the throughput. The rest of the system had to ensure that the print heads were always squirting ink onto the paper. If the print heads were not squirting, we were wasting time. Our customers tended to get upset when their expensive printer paused and hesitated while printing posters because they charge their customers by the square foot. The longer it takes to print the poster, the less money they make.

My primary jobs were to design the controller board for these printers, design the FPGA that was on the controller board, and write the low-level firmware that interfaced with the hardware. Each new product we developed was roughly twice as fast as the previous product, so I constantly had to find new ways to process the image data faster. I started evaluating new microprocessors because the one we were currently using was occasionally making the printer hesitate after each pass of the print heads and would definitely not be sufficient for the next-generation product.

After doing some research and analysis, I found a microprocessor that I felt could handle our processing needs for at least several more future products. I designed a controller board using this part, designed the FPGA logic, and wrote the device drivers and some test code. Everything seemed to be going well. All of the major functional blocks appeared to be working correctly.

The firmware team started working on the project, and, once the team had written enough firmware to make the printer function, it was apparent that this microprocessor appeared significantly slower than the old one. It should have been at least 10 times faster based on clock rate alone, but it also had caches and a DMA controller to further speed things up. The board had copious amounts of high-speed memory, and the FPGA had logic to offload some of the data-processing tasks from the main microprocessor. Something was horribly wrong, and, because I had designed the system, I was the only one who could fix it.

The user's manual for the microprocessor comprised two books with more than 1000 pages each. I grabbed both books and started reading. This incident occurred before PDF files were common, so searching was a manual process. While reading through the debugging section, I came across an interesting feature. This feature set the level of detail about the microprocessor's core and instruction pipeline that is reported to an external debugger.

As I read more about this debugging feature, I discovered that it affects the microprocessor's performance. If you want more detail about what is happening internally, the core slows down. I checked to see what the default setting was and was pleased to discover that maximum detail, slowest core was the reset value. I modified the firmware to turn this feature completely off, and the microprocessor started running at full speed. The printer ran at full speed with no hesitation. My coworkers and I then decided to call this feature the parking brake. EDN

Dan Dull currently works as an electrical engineer for Novo Engineering, a product-development company in Vista, CA.

This Tale is a runner-up in *EDN*'s Tales from the Cube: Tell Us Your Tale contest, sponsored by Tektronix. Read the other finalists' entries at http://bit.ly/Talesfinal_EDN.

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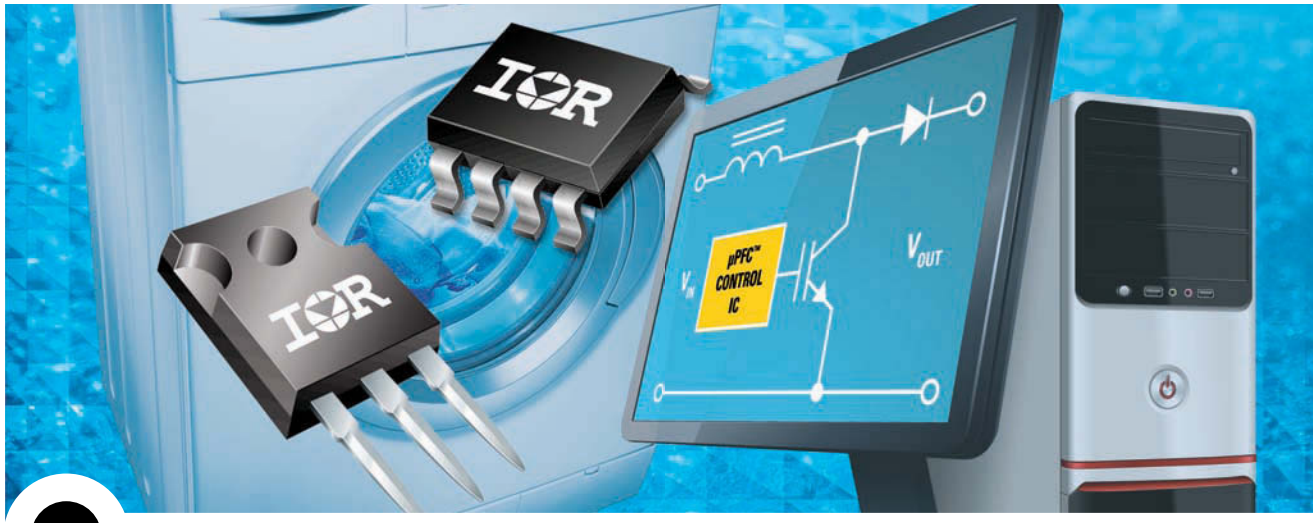

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IRG4(B/IB/P)C30W		12	2.7	TO-220AB; TO-220 FullPak; TO-247AC
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